Thin, Fully Depleted Monolithic Active Pixel Sensor based on 3D Integration of Heterogeneous CMOS Layers

W. Dulinski, G. Bertolone, R. de Masi, Y. Değerli, A. Dorokhov, F. Morel, F. Orsini, L. Ratti, C. Santos, V. Re, X. Wei, and M. Winter

Abstract– **On the way towards fast, radiation tolerant and ultra thin CMOS radiation sensors, we propose new generation of devices based on commercial availability of vertical integration of several CMOS wafers (3D Electronics). In this process, each wafer may be thinned down to about 10 microns end equipped with through-silicon vias (TSV) allowing for electrical interconnection between wafers at a very small pitch (few microns) and with a minimum material budget. The proposed prototype device is a 245x245 pixel array with a pitch of 20 μm, providing active area of 5x5 mm2. In the first silicon layer charge sensing diode and first stage buffer amplifier (source follower) are integrated, using CMOS process on high resistivity epitaxial wafers. Outputs of buffer voltage amplifiers are vertically coupled (through a poly-poly capacitor) to the following stage of processing electronics (charge integration, time continuous shaping and signal discrimination), placed in the second silicon layer (0.13 micron CMOS). The third silicon layer (also 0.13 micron CMOS) is used for implementation of digital (binary) readout with a fast, data driven, self-triggering data flow. After description of the proposed 3D device, an update of results from ongoing tests with the first CMOS MAPS prototype fabricated using high-resistivity epitaxial substrate is provided.**

I. INTRODUCTION

A Monolithic Active Pixel Sensor (MAPS) is a radiation semiconductor sensor which integrates on the same silicon wafer the detector element with the processing electronics. The key element is the use of an N-well/P-substrate diode to collect through thermal diffusion the charge generated by the impinging particle in the thin, undepleted (epitaxial) silicon layer underneath the readout electronics. The device ability to provide high quality tracking of charged (minimum ionizing) particles have been demonstrated on a series of MIMOSA (standing for Minimum Ionizing MOS Active sensor) chip prototypes [1, 2]. Large scale Mimosa26 device (sensitive area of ~2 cm^2) with an integrated sparsifying binary readout has been recently tested and qualified as a sensor for a general purpose beam telescope within EUDET project [3, 4].

Despite these good results, future development and application of today's MAPS generation may suffer from several limitations closely related to its basic working principle. First, using N-well diodes as a charge collection device prohibits the presence of PMOS transistors inside sensing area, severely limiting choice of readout electronics circuitry. In particular, digital cells are allowed on the device periphery only and not within pixels. Second, charge collection through thermal diffusion is slow and induces relatively weak radiation hardness, practical limits being slightly above 10^{12} n/cm^2. Last but not least, the optimal for MIP tracking epitaxial wafers are usually offered by industry in connection with pretty old fashioned CMOS processing.

Rapid progress of microelectronics technology and in particular apparition of so called vertical integration may overcome all mentioned MAPS limitation, still preserving the major advantage: fabrication using standard CMOS processes available through many commercial companies [5]. In this work, we propose novel MAPS architecture based on vertical integration of three wafers coming from two different CMOS suppliers and using two different wafer bonding techniques. We believe that this choice illustrates major trends in industry evolution for the near future. The first ingredient is 3-D integration process offered by Chartered/Tezzaron, with a standard use of TSV (Through-Silicon-Via) and metal-metal (Cu) thermo compression bonding [6, 7]. At present, this process is limited to bonding of two wafers, 0.13 microns feature size each, design constrains being similar to the submission of any CMOS device. The third CMOS wafer will be bonded using DBI$^®$ (Direct Bond Interconnect) technique from Ziptronix [8, 9]. This is low temperature, CMOS compatible, direct oxide bonding for highest density (~1 μm pitch), low mass 3D interconnection. It is claimed to be directly compatible with any modern CMOS process having W-plugs and CMP (chemical mechanical polish) planarization steps. The CMOS process chosen for the fabrication of this third wafer offers high resistivity (~1 kOhm cm) epitaxial substrate to be used as a sensor layer. Two stages of vertical integration process flow for fabrication of the proposed device are shown in figure 1. During the first stage (upper picture), three wafers are put together, the sensor layer is used also as a support of wire bonding pads. In the second stage, the stack may be thinned down to ~50 microns and the bonding pads re-routed to the opposite wafer, taking profit from buried TSV for electrical connections. Such solution allows in principle for the design of edgeless, 4-side buttable sensors.
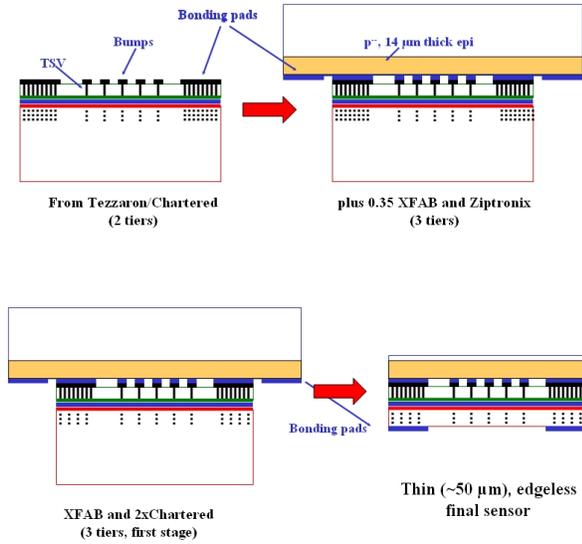
Fig. 1. 3D Integration process flow for the proposed 3-tier device.

II. ARCHITECTURE AND SIMULATION RESULTS OF THE PROTYTYPE 3-TIER DEVICE (STRIPSET)

The proposed prototype device is a 245x245 pixel array with a pitch of 20 μm, providing active area of 5x5 mm^2. A block diagram of a single pixel electronics circuit distributed among three vertically integrated wafers is shown in fig.2. In the first silicon layer charge sensing diode and the input buffer amplifiers (source follower in this case) are integrated, using 0.35 μm CMOS process on high resistivity epitaxial wafers.
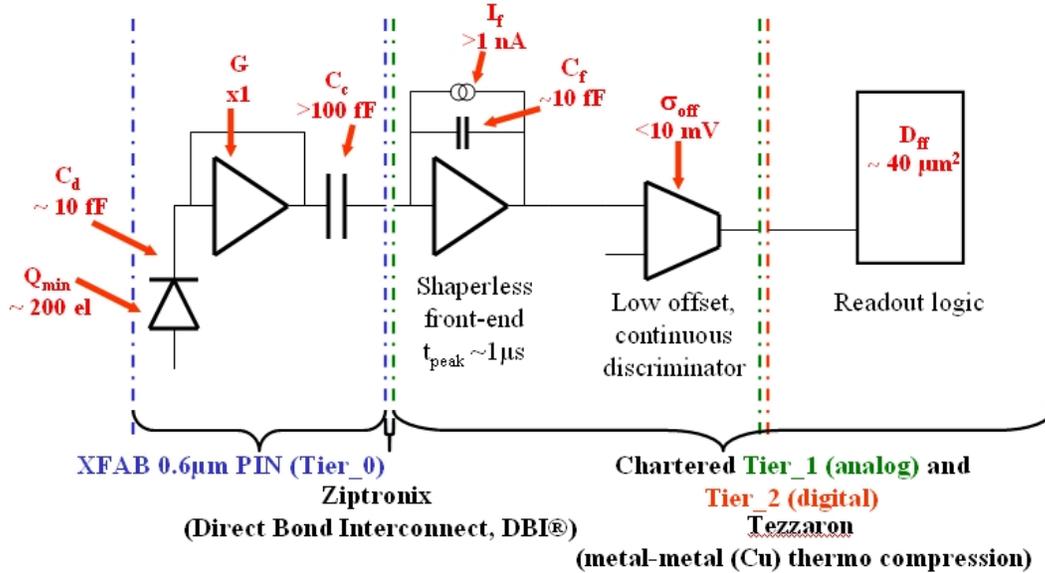
Application of such substrate for particle tracking sensors results in higher signal seen at the seed pixel, reduces strongly cluster multiplicity and in particular, due to fast charge collection (< 5ns), improves radiation hardness with respect to non-depleted CMOS MAPS by at least one order of magnitude. Preliminary tests results of particle tracking with the first CMOS sensor built with high resistivity epitaxial layer process (Mimosa25) will be discussed in the next section.

Outputs of first layer buffer amplifiers are vertically coupled (through poly-poly capacitor) to the following stage of processing electronics (charge integration, time invariant shaping and signal discrimination), placed in the second silicon layer (0.13 micron CMOS). For this stage we have chosen a "shaperless front-end" (SFE) structure already fabricated in similar 0.13 μm process, tested and evaluated [10, 11]. Figure 3 shows result of simulation of entire front end circuit: collecting diode plus a source follower from the first tier followed by shaper amplifier from the second tier. Expected equivalent noise charge (ENC) is less than 15 electrons, for a pulse peaking time of about 500 ns, voltage gain at the discriminator input of 150 μV/e (300 μV/e for the second versions, with 5 fF feedback capacitor) and for total (analog) power dissipation of ~5μW/pixel. In connection with fully depleted, 14 μm thick epitaxial substrate as a charge sensing layer, this should bring very comfortable signal-to-noise ratio of more than 50 (seed pixel Landau most probable) for detection of minimum ionizing particles. Estimated threshold to allow for high detection efficiency of MIP particles is about 150 electrons. Expected time-walk of the discriminator is around 200 ns.

Fig. 2. Block-diagram of the proposed pixel device, showing distribution of different functions among three CMOS wafers (tiers).
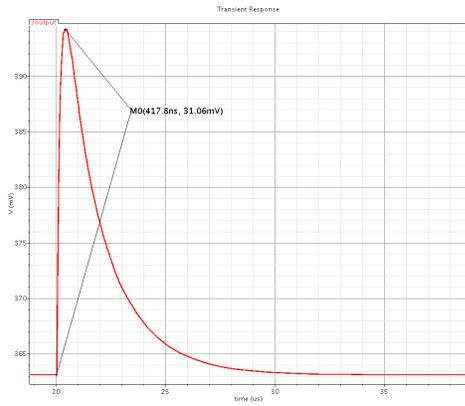
Fig. 3. A simulated pulse at the input of the discriminator, corresponding to injection of 200 electrons at the charge collecting diode in the sensor tier.

Third silicon layer (also 0.13 micron CMOS) is used for implementation of digital (binary) readout, with a fast, data driven, self-triggering data flow (Fig.4). The idea is to read in less than 2 μs the X and Y projection of a hit pattern, latched in the periphery shift registers following a trigger signal set by the first hit pixel. This architecture is proposed and may be useful for applications like a beam telescope, where particle rate may reach MHz range but the most useful events are events having single recorded tracks.
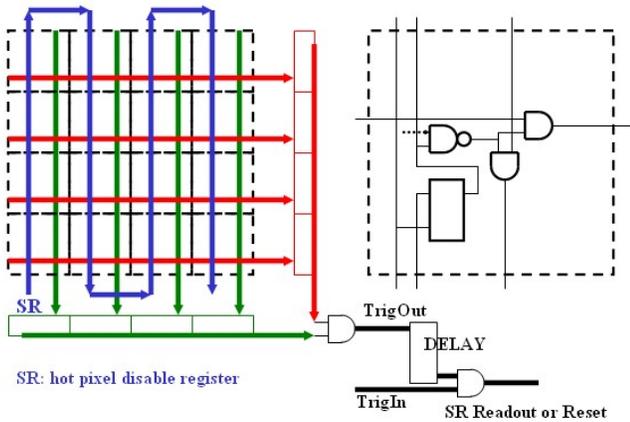

Fig. 4. STRIPSET readout architecture, integrated in the 3-rd tier

The long shift register (snake-like structure in Figure 4) is foreseen for suppression (deactivation) of unwanted noisy pixels, at the same time allowing for programming of any active area shape for trigger application.

III. TRACKING RESULTS WITH FIRST MAPS PROTOTYPE FABRICATED ON HIGH RESISTIVITY EPITAXIAL SUBSTRATE

An update of tests results from the first MAPS (Mimosa25) fabricated on high resistivity epitaxial substrate (~1 kOhm cm) using 0.6 microns CMOS process is presented in this section. Introduction of high-resistivity substrate for MAPS fabrication is considered as a major improvement in their performance and in connection with 3D stacking this will

allow design of a new generation high precision tracking sensors.

Mimosa25 is a small test pixel array, with a very standard and simplified readout electronics based either on classical 3-transistor or on self-biased, 2-transistor pixel cell [12]. In order to study charge collection properties, N-well diodes of different dimensions were implemented and three pitch parameters introduced: 20, 30 and 40 microns. Figure 5 shows charge collection properties for a 20 μm pitch device, with a self-biased diode having 5 x 6.5 μm^2 N-well, measured with Ruthenium beta source before and after neutron irradiation.
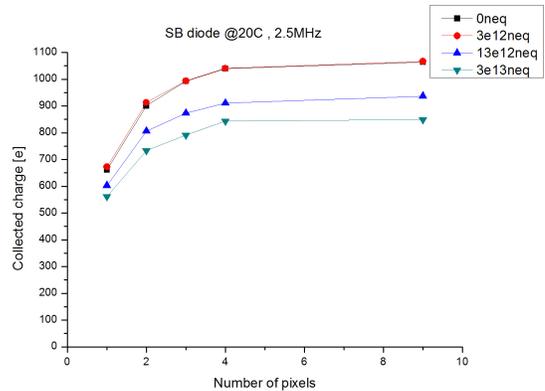

Fig. 5. Charge collected by cluster (m. p. v. of Landau) as a function of number of pixels included in the cluster, before and after neutron irradiation

The charge collected in the seed pixel is more than factor of two larger for the high resistivity layer than for the standard (10 Ohm cm) undepleted layer. The charge spread is also much smaller: >90% of the charge is collected in 3 pixels. Even more important advantage is a faster collection time, which substantially enhances the tolerance to non-ionizing radiation. According to our measurements, the limit of radiation tolerance of MAPS can be therefore extended up to O (10^{14}) n_{eq}/cm^2.

Figure 6 shows signal-over-noise distribution measured with Mimosa25 (the same 20 μm pitch structure) using high energy (120 GeV/c) pion beam. Signal-over-noise ratio for the m. p. v. of the Landau is about 70 before and about 30 after integrated fluence of 3*10^{13} n_{eq}/cm^2. From the bottom plot (zoomed area of the upper one) it is clear that even after such neutron fluence quite comfortable S/N cuts can be applied for the seed pixel signal, without loosing high detection efficiency. At the same time, the track position resolution was measured to be about 3 μm when applying center-of-gravity method for the cluster position calculation and about 4 μm for the simple binary readout.
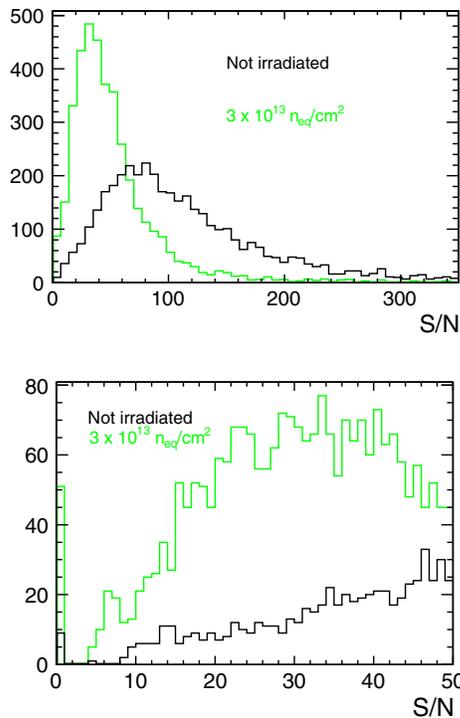
Fig. 6. Landau distribution in S/N units measured with 120 GeV pions.

Beam tests results confirm expected substantial increase of S/N ratio and orders of magnitude improvement of radiation hardness with respect to devices on standard epitaxial layer.

IV. CONCLUSIONS AND PERSPECTIVES

A novel structure for monolithic pixel sensor has been proposed, profiting from 3D integration process offered recently by microelectronics industry. Vertical Integration process allows for tremendous increase of the design architecture flexibility, with an optimal distribution of function for each layer. According to our estimations it is also very efficient approach in order to reduce power consumption, possibly order of magnitude for comparable processing power. This is essential in case of designing very thin detectors, where the most important limitation is coming probably from the power dissipation allowed by the must of low material budget cooling system. Proposed solution may pave a way for the construction of new generation, high precision vertex detectors, approaching also requirements of hadron colliders in term of speed and radiation hardness. Use of new wafer vertical integration technology allow for quite complicated, multi layer structure having equivalent thickness of much less than 100 µm (silicon equivalent) and material budget of the sensor itself may not be the limiting factor for a lot of application. Therefore a new approach to solve yield and reliability problem may be proposed, based on built-in redundancy, i.e. integration of two complete layers and selective powering of chosen area following in-situ testing.

The main goal of presented project is to explore and test all the most promising industrial technologies under development. In addition to the presented sensor, other pixel structures have been submitted for production at the same time, aiming testing of different, more power efficient solutions for analog processing. One of them is based on rolling-shutter architecture, supposing pixel powering only for a short period (typically 100 µW/pixel during 50 ns needed for the signal discrimination), following arbitrary long signal integration time [13]. Second test structure is based on novel, very high gain (1-2 mV/el) and low power (<1µW/pixel) time invariant amplifier-discriminator. All structures are expected to be back from the foundry at the beginning of 2010.

REFERENCES

[1] G. Deptuch et al. "Development of monolithic active pixel sensors for charged particle tracking", Nucl.Instr.Meth. A511 (2003) 240.
[2] W. Dulinski at al. "Optimization of Tracking Performance of CMOS Monolithic Active Pixel Sensors", IEEE Trans.Nucl.Sci.., Vol. 54, No 1, (2007), 284.
[3] J. Baudot et al., "First test results of MIMOSA-26, a fast CMOS sensor with integrated zero suppression and digitized output", IEEE Nuclear Science Symp. Conf. Rec., October 25-31, 2009, Orlando, FL, USA.
[4] T. Haas et al, "A pixel telescope for detector R&D for an international linear collider", Nucl. Instrum. Meth. A, vol. 569, No. 1, Dec. 2006, pp. 53-56.
[5] R. Yarema, "Opportunities for HEP instrumentation using 3D circuits", presented at TIPP'2009, March 12-17, 2009, Tsukuba, Japan.
[6] B. Patti, "Three-dimensional integrated circuits and future of system-on-chip designs", Proc. IEEE, vol. 94, no.6, June 2006, pp. 1214-1224.
[7] R. Yarema, "The first 3D multiproject run for HEP." presented at TWEPPP'2009, September 21-25, 2009, Paris, France.
[8] Q.-Y. Tong, G. Fountain, P. Enquist, "Room temperature SiO2/SiO2 covalent bonding", Appl.Phys.Lett. 89, 042110, 2006.
[9] P. Enquist, "Direct Bond Interconnect for High Energy Particle Detection.", Proceedings of the 7-th International Meeting on Front-End Electronics, May 2009, Montauk.
[10] G. Traversi et al., "CMOS MAPS with pixel level sparsification and time stamping capabilities for applications at the ILC", Nucl. Instrum. Methods, vol. A581, pp. 291-294, 2007.
[11] L. Ratti et al., "Time ivariant analog processor for monolithic n-well CMOS pixel detector", IEEE-NSS 2008 Conference Record.
[12] A. Dorokhov et al., "Improved radiation tolerance of MAPS using a depleted epitaxial layer", Proceedings of the 11th European Symposium on Semiconductor Detectors, Wildbad Kreuth, 2009, to be published.
[13] Y. Degerli et al., "A 3D Integrated Rolling Shutter Mode MAPS with In-Pixel Digital Memory and Delayed Readout", in IEEE Nuclear Science Symp. Conf. Rec., October 25-31, 2009, Orlando, FL, USA.