

## A Portable System For Monolithic Active Pixel Sensors Characterization

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### Introduction

A dynamic research and development program on Monolithic Active Pixel Sensors (MAPS) is going on at LEPSI - IReS since 1999. These devices are candidates for future vertex detectors construction in high energy physics and for radiation imaging in some medical applications within SUCIMA project.

A dedicated test system for MAPS prototypes has been developed. The key feature is flexibility : the same system is used for all prototype test stages, from functional test at wafer reception, until tracking performances measurements on pions beam at CERN.

It is also used for diamond detectors testing, within RD42 CERN collaboration.

PC for Control & Monitoring



#### Analogue Characteristics

- Up to 16 ADC inputs 12 bit
- Sampling frequency up to 20 Mhz

#### Digital Characteristics

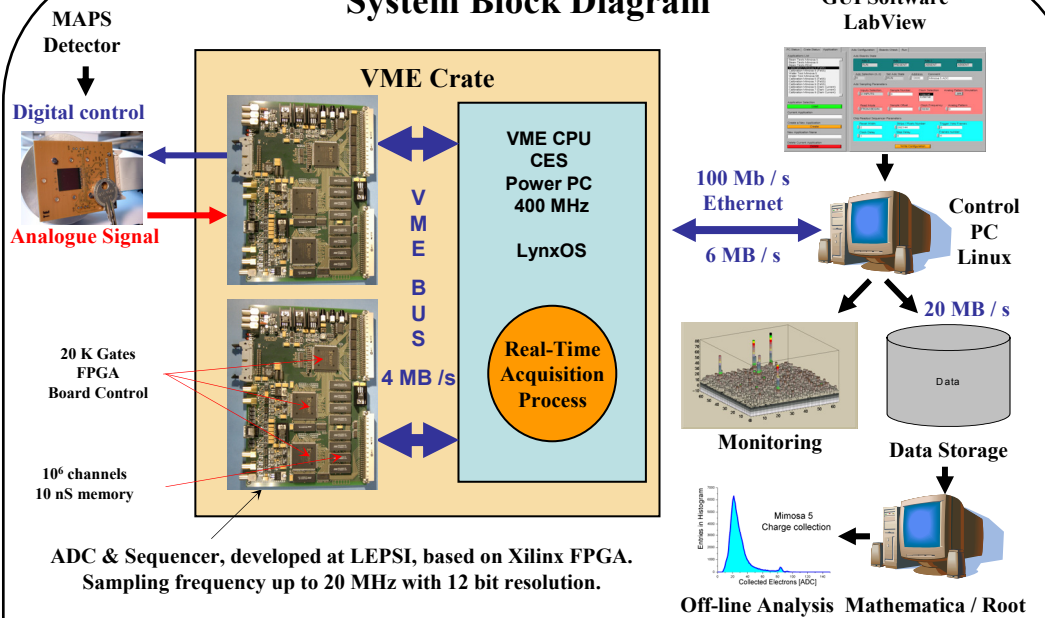
- Trigger input & Pattern generator

#### DAQ Characteristics

- Transfer rate 4 MB / s VME bus
- Handles 128 strips CVD Diamond detectors as well as 10<sup>6</sup> pixels MAPS.

The GUI Labview software allows the user to set measurement parameters. The on-line monitoring makes detector tuning procedure easier. The off-line analysis calculates the prototype performances.

### System Block Diagram

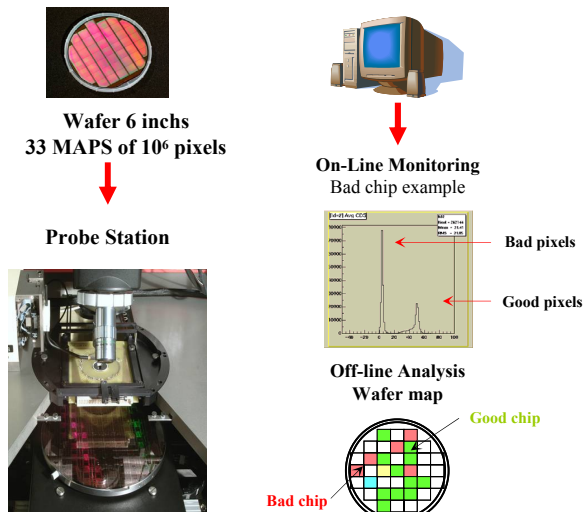


ADC & Sequencer, developed at LEPSI, based on Xilinx FPGA. Sampling frequency up to 20 MHz with 12 bit resolution.

This system is built around a VME DAQ crate. The real-time acquisition process running on the CES PPC, drives the ADC / Sequencer boards. The communication with the GUI control and monitoring PC is based on a RPC client / server protocol. The on-line monitoring samples events in order to display raw data and calculate pedestals and noise. The off-line analysis software processes all events to calculate collected charge distribution.

### Monolithic Active Pixel Sensor Characterization Procedure

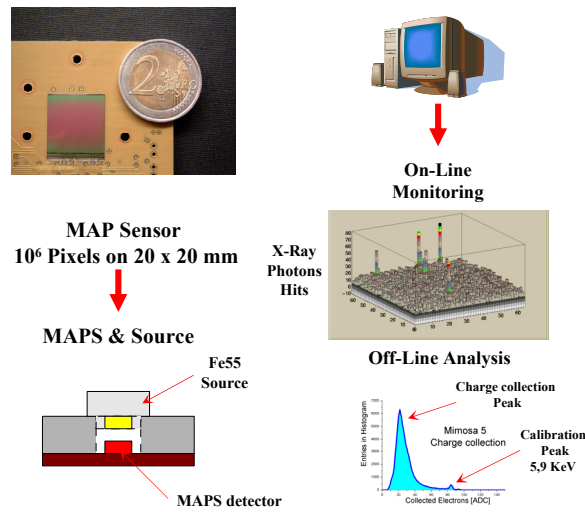
#### On wafer Functional Test



A functional test based on dark current measurement is done in order to detect dead pixels. Off-line processing produces a wafer map of good chips (< 2 % dead pixels).

Up to 660 chips had been tested, each one requiring 40 seconds of acquisition and producing 80 MB of data.

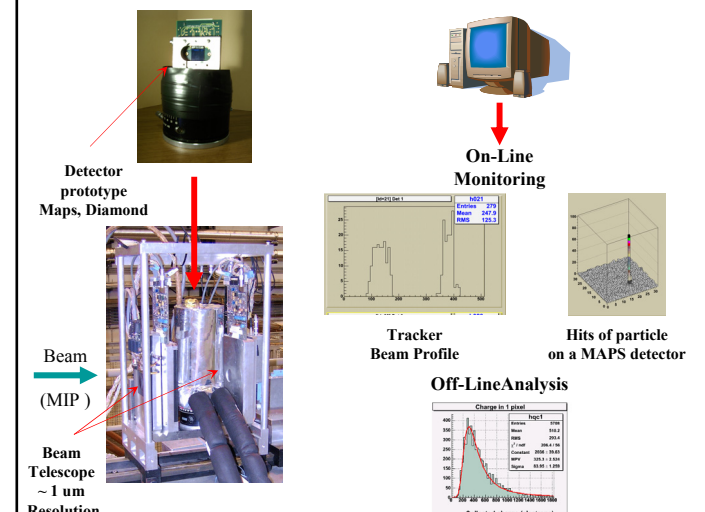
#### Sensor Calibration



X-Ray photons of 5,9 KeV are used for MAPS calibration. The on-line monitoring of hits allows chip parameters tuning. Off-line processing provides average pixels gain.

Statistic requirements are 1000 events for a 10<sup>6</sup> pixels device, translating into 4 GB of data collected in 40 minutes.

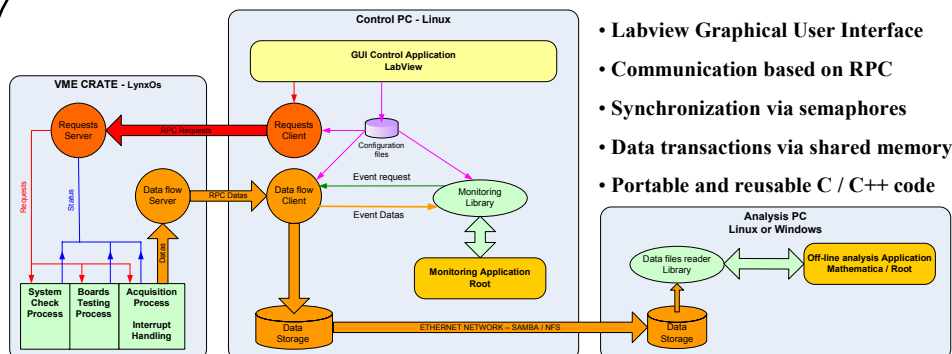
#### Detector Tracking Performances



The prototype is inserted in the beam telescope. On-line monitoring provides beam profile from reference trackers detectors, and shows hits on MAPS. The device tracking parameters are processed off-line.

A sample of 10 000 events is required for a 10<sup>6</sup> pixels MAPS device, translating into 40 GB of data collected in 20 hours of beam.

### Distributed Software Architecture



- Labview Graphical User Interface
- Communication based on RPC
- Synchronization via semaphores
- Data transactions via shared memory
- Portable and reusable C / C++ code

The GUI controls the DAQ process with the Requests client / server. The Data flow server splits events in blocks, send them to the PC by RPC ( Remote Procedure Call ) protocol. The Data flow client builds events from blocks, writes them to hard disk. It also provides events, via a shared memory, to monitoring application requests.

Raw data format is handled by specific libraries, which allow transparent access by Mathematica or Root analysis tools to the events files.

### New Generation ... USB 2.0 Bus

#### Analogue Characteristics

- Up to 16 ADC inputs 12 / 14 bits
- Sampling frequency up to 40 / 100 Mhz

#### Digital Characteristics

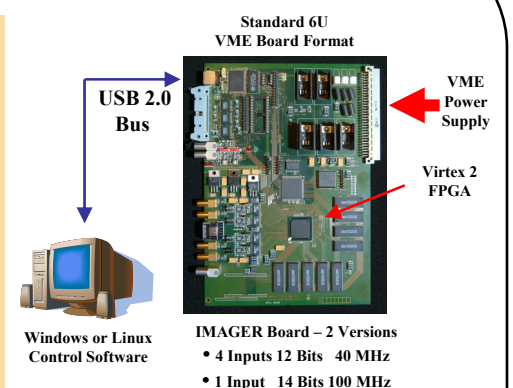
- Trigger input & Pattern Generator

#### DAQ Characteristics

- Transfer rate 15 MB / s USB 2.0 bus

#### On-board data processing

- Pedestals subtraction, zero suppression



In order to increase the system integration, the IMAGER board has been developed. It allows implementation of on-line data processing algorithms. The architecture is based on USB 2.0 bus for data transfer and a Virtex 2 (10<sup>6</sup> gates) FPGA as board controller. This board has been integrated in the modular DAQ software, which also runs under Windows.