Development of CMOS pixel sensors for tracking and vertexing in high energy physics experiments

Serhiy Senyukov (IPHC-CNRS Strasbourg) on behalf of the PICSEL group
Outline

• CMOS Pixel Sensors (CPS):
  – Principle of operation
  – Advantages vs. limitations
  – State of the art
• Future projects
• Current developments in IPHC
• Prototype test results (preliminary)
• Conclusions & outlook
CPS – principle of operation, advantages vs. limitations

• Sensitive volume and readout chain in a single silicon die:
  – High granularity (pitch ~ 20 µm)
  – Low material budget
    (50 µm of Si \( \rightarrow \) ~ 0.3% \( X_0 \) per layer)
  – Low production cost (large scale commercial providers and no bump bonding needed)

• Optimal choice for the low-\( p_T \) tracking and vertexing (i.e. heavy flavors)

• Radiation hardness and readout speed are determined by the CMOS process parameters i.e.:
  – feature size \( \rightarrow \) TID hardness
  – epi-layer resistivity \( \rightarrow \) NIEL hardness
State of the art: Ultimate-2 for STAR-PXL

- First CPS in the HEP experiment:
  - AMS 0.35 µm process
  - Pixel pitch: 20.7 µm (960×928 pixels)
  - Rolling shutter readout
  - Integration time: < 200 µs
  - TID: 150 kRad
  - NIEL: $3 \times 10^{12} \text{n}_{\text{eq}}/\text{cm}^2 \ @ \ 35 \ ^\circ \text{C}$
  - Chip thickness: 50 µm $\rightarrow$ 0.37 % $X_0$ per layer

- 3 out of 10 sectors installed on 8th May 2013
- Commissioning with pp and light ion collisions in May – June 2013.
- More details in the talk by M. Szeleznia on Wed. 9th October
## New projects – new challenges

<table>
<thead>
<tr>
<th></th>
<th>Spatial resolution [µm]</th>
<th>Integration time (µs)</th>
<th>TID (MRad)</th>
<th>NIEL ($n_{eq}/cm^2$)</th>
<th>Temp (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>~5</td>
<td>200</td>
<td>0.15</td>
<td>$3\times10^{12}$</td>
<td>35</td>
</tr>
<tr>
<td>ALICE-ITS</td>
<td>~5</td>
<td>10-30</td>
<td>0.7</td>
<td>$10^{13}$</td>
<td>30</td>
</tr>
<tr>
<td>CBM-MVD</td>
<td>~5</td>
<td>10-30</td>
<td>10</td>
<td>$10^{14}$</td>
<td>&lt;0</td>
</tr>
<tr>
<td>ILD-VXD</td>
<td>~3</td>
<td>≤10</td>
<td>~0.1</td>
<td>~$10^{11}$</td>
<td>30</td>
</tr>
</tbody>
</table>

- AMS 0.35 µm process cannot satisfy the requirements of the future projects
- Another CMOS process is needed with
  - Smaller feature size to
    - Increase TID hardness (thinner gate oxide)
    - Allow more sophisticated and faster readout
  - Higher resistivity of the epitaxial layer to
    - Increase NIEL hardness (more depletion, less sensitive to the charge traps)
TowerJazz® CMOS process

- Feature size: 0.18 µm
- Thick epitaxial layer: 18-40 µm, 1 < ρ < 6 kΩ*cm
- Six metal layers
- Deep P-well option (P-layer underneath N-well protecting from parasitic charge collection) allows usage of PMOS transistors
- Stitching option
2012: first validation of the process

- 2 prototypes tested in the lab and at CERN-SPS
- Radiation hardness of the process proven:
  - Det. efficiency \(\sim 98\% \) @30 °C after \(1\) MRad + \(10^{13}\) n_{eq}/cm\(^2\)

Main issue:
- Non-gaussian tail of the noise distribution due to the Random Telegraphic Signal (RTS)

arXiv:1305.0531
Development of the full scale chips

**MISTRAL**
- In-pixel CDS
- Column-level discriminator
- Rolling shutter readout
- 2 rows read out in parallel
- Integration time: 30 µs
- Power: < 200 mW/cm²

**ASTRAL**
- In-pixel CDS
- In-pixel discriminator
- Rolling shutter readout
- 2 rows read out in parallel
- Integration time: 15 µs
- Power: ≤ 100 mW/cm²

**common zero suppression logic (SUZE 02)**
- 2D Cluster search
- Encoding of 4 × 5 pixels windows
- Output data rate ~ 1 Gbit/s
March 2013 engineering run

- Joint effort in collaboration with CERN and RAL (UK)
- 6 most important chips:
  - **MIMOSA 22THR(A1/A2/B):**
    - RTS noise mitigation
    - 2-row readout validation
  - **AROM-0:** ASTRAL in-pixel circuitry validation
  - **SUZE 02:** zero suppression
  - **MIMOSA 34:** optimization of pixel size and design, epitaxial layer thickness and resistivity

Actual reticle 21.5x31 mm²
Laboratory tests: noise

- **MIMOSA 22 THR-A** – RTS noise mitigation through the gate size of the input transistor
  - RTS noise tail is suppressed ($TN \approx 17 \text{ e}^{-}$)

- **MIMOSA 22 THR-B** – double row readout via end-of-column discriminators
  - FPN increase due to the coupling ($3 \rightarrow 5 \text{ e}^{-} \text{ ENC}$)
Beam tests:
Detection efficiency & fake hit rate

- **MIMOSA 22THR-A1** tested with the ~5 GeV/c electron beam at DESY in Aug 2013
  - Result: in the threshold range of $(5-8) \times \sigma_{\text{noise}}$
    - Detection efficiency $\varepsilon_{\text{det}} \geq 99.5\%$
    - Fake rate $\sim 10^{-5}$ for the pixels with RTS mitigation (S1, S2)
- To be confirmed after irradiation
Spatial resolution vs. pixel pitch

- Measurement was performed with **MIMOSA 34** chip at DESY electron beam
- Pixels sizes tested: 22×30, 22×33, 22×44, 22×66 µm²
- “Analog” resolution via 12-bit signal encoding:
  - ~2.5 µm for 22×33 µm²
  - ~3.5 µm for 22×66 µm²
- “Binary” resolution after conversion to 1-bit clusters:
  - < 5 µm for 22×33 µm²
  - < 7 µm for 22×66 µm²
- Results compatible with previous chips.
AROM-0: in-pixel discriminators

- 3 versions of the in-pixel discriminator
- 4 32×32 pixel matrices with single row readout
- 2 16×16 pixel matrices with double row readout
- Chip tested in the lab
- Noise estimated from the transfer function (S-curve)

16×16 matrix
Double row readout
TN = 1.52 mV
FPN = 0.45 mV
X1.5 higher than target
To be improved
Conclusions & outlook

• TowerJazz 0.18 µm CMOS process is chosen for the on-going CPS developments for ALICE ITS upgrade and CBM-MVD

• Upstream and downstream parts of the final architectures (MISTRAL/ASTRAL) will be validated in 2013

• 2014-15 – production of the first full scale (~1 cm²) prototypes

• 2015-16 – production of the final chips for ALICE-ITS and CBM-MVD

• 2017-19 – adaptation to the ILD requirements
Thank you for your attention
Cluster multiplicity

MIMOSA 34, binary emulation, cluster multiplicity

Graph showing cluster multiplicity for different pixel sizes and diode areas at $T_{\text{cool}} = 30^\circ\text{C}$.