Introduction to CMOS Pixel Sensors

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OUTLINE

• Main features of CMOS pixel sensors
  ▶ motivation ▶ principle: sensing & read-out ▶ limitations ▶ hit characteristics

• Achieved performances
  ▶ means of evaluation ▶ beam test characterisation ▶ sources of performance degradation

• Applications
  ▶ system integration aspects ▶ subatomic physics apparatus

• Outlook
  ▶ 2D sensors ▶ 3D sensors

• Summary
The Quadrature of the Vertex Detector

- CMOS pixel sensors offer the perspective of "combining the extremes" (ultimately !)

- Several labs develop CMOS pixel sensors:
  - Italy (Univ., INFN), UK (RAL), CERN,
  - Germany (Heidelberg, Bonn, ...), USA,
  - France (IPHC, Saclay), ...

- CMOS Pixel Sensors chosen/envisaged by growing number of subatomic physics experiments:
  - STAR at RHIC/BNL: commissioning
  - ALICE at LHC/CERN: under development
  - CBM at FAIR/GSI: under development
  - ILC: option
  - Etc.

- Variety of applications besides subatomic physics:
  - dosimetry, hadrontherapy, $\gamma$ & $\beta$ counting, ...
CMOS Technology

- C.M.O.S. ≡ Complementary Metal-Oxide-Semiconductor

- CMOS pixel sensors exploit the fabrication processes used in industry for mass production of integrated circuits:
  - micro-processors, micro-controller, RAM, ...
  - cell phones & cameras, lap tops, cars, ...

- CMOS fabrication mode:
  - $\mu$-circuit lithography on a substrate
  - proceeds through reticules ($\sim 2\times2 \rightarrow 2\times3 \text{ cm}^2$) organised in wafers (typically 8")
Main Features of CMOS Sensors

- P-type low-resistivity \((O(10)\Omega \cdot cm)\) Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    \(Q \sim 70–80\ e\cdot h/\mu m \implies \text{signal } \lesssim 1000\ e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)
    \(\implies\) continuous signal sensing (no dead time)

- Prominent advantages of CMOS sensors:
  - \textbf{grainularity}: pixels of \(\lesssim 10 \times 10\ \mu m^2\) \(\implies\) high spatial resolution (e.g. \(\lesssim 1\ \mu m\) if needed)
  - \textbf{low material budget}: sensitive volume \(\sim 10 - 20\ \mu m\) \(\implies\) total thickness \(\lesssim 50\ \mu m\)
  - \textbf{signal processing} \(\mu\text{circuits integrated in the sensors}\) \(\implies\) compacity, high data throughput, flexibility, etc.
  - \textbf{industrial mass production} \(\implies\) cost, industrial reliability, fabrication duration, multi-project run frequency, technology evolution, ...
  - \textbf{operating conditions}: from \(\ll 0^\circ C\) to \(\gtrsim 30-40^\circ C\)

\(\implies\) Thinning down to \(\sim 30\ \mu m\) permitted
Basic Read-Out Architecture

Based on 3 transistor cell

$V_{Q, integr}$

$V_{reset}$

$\Delta v_{typ} \propto I_{leak}$

$\Delta v_{sig} \propto Q_{signal}$

Integration time

 ADC

Array of pixels

High-speed

Analog read-out

& storage

Low power – only significant draw at readout edge

Pixel Array: Column select – ganged row read

Pixel

Collection Electrode

Restores potential to collection electrode

Rest on 3 transistor cell

Source follower buffering of collected charge

Row Bus Output

M1

M2

M3

Column Select

Gnd

Vdd

Vdd

Reset

Resets circuit

$t_{fr1}$

$t_{fr2}$

$t_{reset}$
CMOS Pixel Sensors: Read-Out Architectures

• Signal sensing and read-out are decoupled:
  ※ signal sensing (charge collection) is continuous (no dead time)
  ⇒ signal read-out may be performed in various ways, independently of charge collection

• Signal processing alternatives:
  ※ self-triggered: only fired pixels are (randomly) read-out  ≡ hybrid pixels
  ※ rolling shutter (less power consumption): read-out of all pixels (A or D), followed by sparsification outside of sensitive area
  ※ snap-shot: requires 2 consecutive read-outs, with 1 used for average noise subtraction (rather suited to light imaging due to up to 50 % dead time)

• Signal transfer alternatives:
  ※ continuous: permanent output to outside world
  ※ intermittent: signal stored on chip until read-out sign is provided  ← event based trigger or beam time structure (ILC)
Overview of Rolling Shutter Architecture

- **Sensor organisation:**
  - Signal sensing and analog processing in pixel array
  - Mixed and Digital circuitry integrated in chip periphery
  - Read-out in rolling shutter mode
    (pixels grouped in columns read-out in //)
  - trend: increase functionalities inside pixels

- **Main consequences:**
  - **Read-out speed:**
    - integration time
    - nb of pixels × pixel read-out time (O(100 ns))
  - **Power consumption:**
    - limited inside the pixel array to the row(s) being read out
  - **Material budget:**
    - peripheral band(s) for mixed+digital circuitry, insensitive to impinging particles
    - ~ 10 % of chip surface
  - **Time stamp:**
    - each row encompasses a specific time intervalle
    - adapt (exploit with) track reconstruction code
Signal Sensing & Processing Architectures

- **Main sensing and read-out micro-circuit elements:**
  - in-pixel conversion of charge into electrical signal (e.g. voltage) with average noise subtraction
  - signal discrimination (in perspective of zero-suppression)
  - discriminator output encoding (sparsification with charge encoding)
  - data transmission logic → connection with the outside world

- **In-pixel μcircuitry:**

```
<table>
<thead>
<tr>
<th>basic read-out</th>
<th>pre-amp + &lt;noise&gt; subtraction</th>
<th>pre-amp + shaper + discriminator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>outside chip</td>
<td>chip periphery</td>
</tr>
<tr>
<td>Reduction</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
Limitations of the Technology

- Very thin sensitive volume
  ⇒ impact on signal magnitude (mV !) ⇒ very low noise FEE required

- Sensitive volume only partly depleted
  ⇒ negative impact on radiation tolerance & speed but positive on $\sigma_{sp}$ (charge spread)
  ▶ tendency : high-resistivity epitaxial layer ⇒ improved radiation tolerance (SNR)

- Commercial fabrication
  ⇒ fabrication parametres (doping profile $\rightarrow$ epitaxial layer, number of metal layers, etc.)
  not optimal for charged particle detection (optimised for commercial items):
    * real potential of CMOS pixel sensors not exploited (yet !)
    * choice of process for HEP often driven by epitaxial layer characteristics (governs signal),
      at the expense of the FEE circuitry parametres (feature size, nb of Metal Layers)

- Use of P-MOS transistors inside pixel array restricted in most processes
  ⇒ limited signal processing functionnalities inside (small) pixels (most performed on sensor periphery)
  ▶ tendency : buried P-well techno. ⇒ allows use of P-MOS transistors (watch charge coll. eff. !)
Hit Characteristics

- Standard processes: charges diffuse thermally
  - \( \lesssim 10^3 \) e\(^-\) shared among \( \sim 10\text{-}15 \) pixels per cluster
  - typically \( \lesssim 200/300 \) e\(^-\) (MPV) in seed pixel

- High-resistivity epitaxy (O(k\(\Omega\cdot cm\))): larger charge sensing volume
  - less diffusion \( \Rightarrow \) less pixels/cluster (typically \( \lesssim 4 \))
  - larger charge collected/pixel (e.g. \( \sim 500 \) e\(^-\)) \( \Rightarrow \) higher SNR

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Total cluster charge (5x5 pixels)

Pixel multiplicity vs Threshold

For comparison: standard CMOS technology, low resistivity P-epi

Depletion zone

high resistivity (1kOhm\(\cdot\)cm) P-epi: size of depletion zone size is comparable to the P-epi thickness!
Calibration of Charge-to-Voltage Conversion Factor

- **Goal**: establish a well defined correspondence between the measured sensor output voltages and the amplitude of the charge collected by each diode.

- **Mean**: use radioactive sources emitting particles with adapted and well defined energy.

- **Ex**: $^{55}$Fe source
  - emits X-Rays with 5.9 keV ($\sim 90\%$) or 6.49 keV ($\sim 10\%$).
  - X-Rays interact with Si atoms through photo-electric effect:
    - the ejected p.e. carries $\sim 100\%$ of the X-Ray energy ($e^{-}$ binding energy ...).
  - the p.e. creates eh pairs at the expense of $\sim 3.6$ eV per pair:
    - $5900/3.6 \approx 1640$ eh pairs ($6490/3.6 \approx 1800$ eh)

- **Calibration with $^{55}$Fe X-Rays**
  - a small fraction of X-Rays impinge sensor near sensing diode:
    - nearly all $e^{-}$ created get collected by nearby sensing diode.
  - the charge distribution observed on the ADC scale exhibits 2 peaks.
Main Sources:

- in pixel: sensing diode capacitance
- in pixel: leakage current collected by sensing diode
- outside pixel: signal processing micro-circuits

Tricks to minimise the noise:

- maximal amplification inside pixel
  ⇒ minimises impact of the noise of signal processing micro-circuits
- operate chip with short integration time
  ⇒ minimises integrated leakage current
- operate chip at low temperature
  ⇒ minimises thermal noise
M.I.P. Detection Performance Evaluation

- **Laboratory:**
  - test steering & read-out functionalities (e.g. pattern generator)
  - evaluate charge collection efficiency & noise (\(^{55}\)Fe, light)
  - assess charge-to-voltage conversion factor (\(^{55}\)Fe)
  - estimate "m.i.p." detection efficiency with \(\beta\) (\(^{106}\)Ru)

- **Particle beams:**
  - typically \(\sim 100\) GeV/c \(\pi^-\) at CERN-SPS (not really m.i.p.)
    - \(\Rightarrow\) minimise multiple scattering
  - install chip to test inside beam telescope (EUDET BT)
  - determine:
    - detection efficiency (and SNR)
    - fake hit rate (and noise)
    - single point resolution
    - etc.
CMOS Pixel Sensors: State of the Art

CMOS 0.35 μm OPTO technology
Chip size: 13.7 x 21.5 mm²

- Testability: several test points implemented all along readout path
  - Pixels out (analogue)
  - Discriminators
  - Zero suppression
  - Data transmission

- Pixel array: 576 x 1152, pitch: 18.4 μm
- Active area: ~10.6 x 21.2 mm²
- In each pixel:
  - Amplification
  - CDS (Correlated Double Sampling)

- Row sequencer
- Width: ~350 μm

- 1152 column-level discriminators
  - Offset compensated high gain preamplifier followed by latch

- Zero suppression logic

- Reference Voltages Buffering for 1152 discriminators

- I/O Pads
  - Power supply Pads
  - Circuit control Pads
  - LVDS Tx & Rx

- Current Ref.
- Bias DACs
- Readout controller
- JTAG controller
- Memory management
- Memory IP blocks
- PLL: 8b/10b optional

TWEPP-2010
**M.I.P. Detection Efficiency & Fake Hit Rate**

- **Motivation**: find a sensor working point with high detection efficiency and marginal contamination from noise fluctuations (fake hits)

- **Detection efficiency**
  - fraction of tracks reconstructed in telescope which are also reconstructed in the sensor
  - study as function of discriminator threshold
  - a high threshold may harm detection efficiency \( \Rightarrow \) Trade-off!

- **Fake hit rate**
  - fraction of noise fluctuations which pass the discriminator threshold
  - study as a function of discriminator threshold
  - a high threshold is best to keep fake rate marginal, but ... (typically \( \lesssim 10^{-3/-4} \))
• Compare position of impact on sensor surface predicted with BT to position of hit reconstructed with sensor under test:
  clusters reconstructed with eta-function,
  exploiting charge sharing between pixels

• Impact of pixel pitch (analog output):
  \( \sigma_{sp} \sim 1 \, \mu m \) (10 \( \mu m \) pitch) \( \rightarrow \lesssim 3 \, \mu m \) (40 \( \mu m \) pitch)

• Impact of charge encoding resolution:
  \( \triangleright \) ex. of 20 \( \mu m \) pitch \( \Rightarrow \sigma_{sp}^{\text{dig}} = \text{pitch}/\sqrt{12} \sim 5.7 \, \mu m \)

<table>
<thead>
<tr>
<th>Nb of bits</th>
<th>12</th>
<th>3-4</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>measured</td>
<td>reprocessed</td>
<td>measured</td>
</tr>
<tr>
<td>( \sigma_{sp} )</td>
<td>( \lesssim 1.5 \mu m )</td>
<td>( \lesssim 2 \mu m )</td>
<td>( \lesssim 3.5 \mu m )</td>
</tr>
</tbody>
</table>
Radiation Tolerance

- **Introductory remarks:**
  - still evolving (csq of CMOS industry process param. evolution)
  - CMOS technology expected to tolerate high ionising radiation doses (≫ 10 MRad), in particular with $T < 0^\circ$C & short $t_{integ}$
  - main a priori concern: NON-ionising radiation (in absence of thick depleted sensitive volume)

- **Influence of pixel pitch:**
  - fig: all measts done with low resistivity epitaxial layer, but 1 high density sensing diodes (≡ small pitch)
    improves non-ionising radiation tolerance

- **Influence of epitaxial layer resistivity:**
  - ex: 400 $\Omega \cdot cm$ & $O(1)$V depletion voltage
  - trend: $\gtrsim 1 k\Omega \cdot cm$ & $\gtrsim 10$ V

⇒ Tolerance to $\gtrsim 10^{14-15} \text{n}_{eq}/cm^2$ seems achievable
Sensor Integration in Ultra Light Devices

- "Useful" sensor thickness $\lesssim 30 \mu m \Rightarrow$ opens up new possibilities w.r.t. thicker sensors
  - coarse thickness of sensors (e.g. STAR-PXL) is 50 $\mu m$

- STAR-PXL ladder (room temperature, single-end supported):
  - total material budget $\simeq 0.37 \% X_0$:
    - 50 $\mu m$ thin sensors $\simeq 0.05 \% X_0$
    - flexible cable $\simeq 0.07 \% X_0$
    - mechanical support $\simeq 0.2 \% X_0$
    - adhesive, etc. $\simeq 0.05 \% X_0$

- Double-sided ladders with $\sim 0.2-0.3 \% X_0$:
  - manifold bonus: compactness, alignment, redundancy, pointing accuracy (shallow angle), fake hit rejection, etc.

- Unsupported & flexible ladders with $\lesssim 0.15 \% X_0$
  - 30 $\mu m$ thin CMOS sensors mounted on thin cable & embedded in thin polyimide $\Rightarrow$ suited to beam pipe?
Examples of Applications in Subatomic Physics

- **Beam telescopes**:
  - EUDET (FP-6 / 2006-2010) : 6 planes with $1 \times 2 \, \text{cm}^2$ sensors
  - AIDA (FP-7 / 2011-2015) : $\geq 3$ planes with $4 \times 6 \, \text{cm}^2$ sensors

- **Vertex detectors**:
  - STAR-PXL at RHIC : 2 layers
  - CBM-MVD at FAIR/GSI : 2-3 stations
  - ALICE-ITS at LHC : 3 inner layers
  - FIRST at GSI (p/C PMMA x-sec) : 4 stations
  - option for ILD-VTX at ILC : 3 double-layers

- **Trackers ("large pitch")**:
  - BES-III at BEPC
  - ALICE-ITS at LHC : 4 outer layers ($\lesssim 10 \, \text{m}^2$)
  - in general : trackers surrounding vertex detectors

- **EM calorimetres** : SiW calorimetre
  - generic R&D on TRACAL
Perspectives: Fast 2D sensors

- Evolve towards feature size $<< 0.35 \mu m$:
  - $\mu$circuits: smaller transistors, more Metal Layers, ...
  - sensing: quadruple well, depleted sensitive volume, ...

- Benefits:
  - faster read-out $\Rightarrow$ improved time resolution
  - higher $\mu$circuit density $\Rightarrow$ higher data reduction capability
  - thinner gates, depletion $\Rightarrow$ improved radiation tolerance

- On-going R&D (examples):
  - **APSEL** sensor (130 nm) for future Vx Det.:
    - in-pixel pre-amp + shaping + discrim.
    - sensing through buried n-well
    - shallow n-well hosting P-MOS T
  - **TJSC** project (180 nm) for ALICE-ITS upgrade:
    - high-resistivity, 18-40 $\mu m$ thick, epitaxy
    - deep P-wells hosting P-MOS T

- Main limitations:
  - VDSM technologies not optimised for analog $\mu$circuits (low V !) $\Rightarrow$ reliability
  - conflict between speed (e.g. 10 ns) and granularity (e.g. $20 \times 20 \mu m^2$ pixels)

$\Rightarrow$ **Natural trend**: chip stacking
Using 3DIT to reach Ultimate CMOS Sensor Performances

- 3D Integration Technologies allow integrating high density signal processing \( \mu \)circuits inside small pixels by stacking (\( \sim 10 \ \mu m \)) thin tiers interconnected at pixel level.

- 3DIT are expected to be particularly beneficial for (small pixel) CMOS sensors:
  - combine different fab. processes \( \Rightarrow \) chose best one for each tier/functionnality
  - alleviate constraints on peripheral circuitry and on transistor type inside pixel, etc.

- Split signal collection and processing functionalities:
  - Tier-1: charge sensing
  - Tier-2: analog-mixed \( \mu \)circuits
  - Tier-3: digital \( \mu \)circuits

- The path to nominal exploitation of CMOS pixel potential:
  - fully depleted 10-20 \( \mu m \) thick epitaxy \( \Rightarrow \) \( \lesssim 5 \) ns collect. time, rad. hardness \( > \) Hybrid Pix. Sensors ???
  - FEE with \( \leq 10 \) ns time resolution \( \Rightarrow \) solution for CLIC & HL-LHC specifications ???

- 3DIC \( \equiv \) consortium coordinated by FermiLab has already produced 1st generation of chips
• CMOS sensor technology has become mature for high performance vertexing and tracking
  * most relevant for specifications governed by granularity, material budget, power consumption, cost, ...
  * excellent performance record with beam telescopes (e.g. EUDET project)
  * 1st vertex detector experience will be gained with STAR-PXL, starting data taking in a few weeks ...
  * new generation of sensors under development for experiments > 2015 (including trackers & calo.)
    ALICE-ITS upgrade (see also talk of W. Snoeys), CBM-MVD (FAIR), ..., ILC VD (?), ...

• Technology full potential still far from being exploited
  (despite improvement due to high-resistivity epitaxial layer processes)

• Evolution of industry opens the door to 2 ”natural” steps
  towards the ”ultimate” performances of the technology :
  * fast 2D sensors based on VDSM CMOS technologies may allow for \( \lesssim O(1) \ \mu s \), \( \gg 10 \text{ MRad} \)
  * 3D chips are expected to ”exhaust” the technology potential, but there is still a rather long way to go
    \( \Rightarrow \) may lead to fast & rad. hard devices suited to HL-LHC & CLIC