Status and Plans of ASTRAL & MISTRAL Developments

M.W. / 4 June 2013
PICSEL-ALICE team of IPHC

Outline

- Reminder: objectives and development plans
- Questions addressed in the forthcoming prototypes
- 2014-2016 Work Plan
- Summary
Reminder : Main objective

★ EXTEND THE STAR-PXL CPS (MIMOSA-28) CONCEPT :

✿ rolling shutter read-dout
✿ in-pixel ampli + clamping
✿ pixels organised in columns ended with discrim.
✿ discriminators followed by SDS μcircuitry
✿ output buffers storing the SDS results
✿ JTAG for param. setting and control

★ PROMINENT CHANGES WRT MIMOSA-28 :

✿ radiation tolerance improvement by factor of $\sim 3$
  $\rightarrow$ moving from AMS-0.35 to TJSC-0.18 process
✿ read-out speed by factor $\gtrsim 6$ :
  ○ step 1 (MISTRAL) : $30 \, \mu s$ & $< 350 \, mW/cm^2$
    $\rightarrow$ 2 rows r.o. simultaneously & less pixels per column
  ○ step 2 (ASTRAL) : $15 \, \mu s$ & $\lesssim 150 \, mW/cm^2$ (or $< 10 \, \mu s$ & $\sim 200 \, mW/cm^2$)
    $\rightarrow$ in-pixel discrim. (and possibly 4 rows r.o. simultaneously $\Rightarrow$ pixel size ?)
    $\Rightarrow \Rightarrow \Rightarrow$ digital power is $\sim 3/4$ of total consumption
### General Features of the Sensor (Inner Layers):

- 3 neighbouring independent blocks (\( \equiv \) FSBB): \( \sim 1 \text{ cm}^2 \)
- FSBB:
  - Pixel array organised in columns (rolling shutter r.o.)
    - 2 options: in-pixel or end-of-column discriminators
  - Sparse data scan on chip periphery
  - 4 output buffers (512 x 32 bits each)
- 3 FSBB (160 MHz) outputs multipl. in 1 (\( \gtrsim 1 \text{ Gbit/s} \)) LVDS output

### Main Development Steps:

- 2011/12: pixel design \( \triangleright \) dimensions vs resolution, rad. tol., etc.
- 2012/13: Validation of main components of global architecture \( \triangleright \) pixel array, sparsification circuitry & output buffers
  - Optimisation of pixel design (incl. noise reduction)
- 2013/14: FSBB design combining all components
- 2015/16: Final sensor design

### Pending Issues:

- ASTRAL (15 \( \mu s \); less advanced) or MISTRAL (30 \( \mu s \); less innovative)
- Design of signal transmission circuitry
- Chip design for outer layers: extended ASTRAL preferred (\( \lesssim 70 \text{ mW/cm}^2 \) ?)
Summary of Overall Strategy

- 2 different streams followed in parallel in order to match the timescale:
  - **Main stream**: fast track devt, still not optimised nor providing the fastest read-out
  - **Side stream**: main stream design optimisation and alternative accelerated read-out design

- **Main stream**:
  - end of column discriminators (2 / col.) \(\Rightarrow\) 30 \(\mu s\) read-out time (MISTRAL)
  - fixed parameters of sparsification and memorisation circuitry

- **Side streams**:
  - optimisation path: staggered diodes, in-pixel & sparsification circuitry optimisation, ...
  - acceleration path: in-pixel discriminator (AROM) architecture devt \(\Rightarrow\) 15 \(\mu s\) read-out time (ASTRAL)

- **Main chip components addressed by R&D**: Charge sensing node (CS), In-pixel ampli+clamping (AC), Discriminator (DI), Zero-suppression circuitry (ZS), Output buffers (OB), Transfer circuitry (DT), Steering circuitry (SC)

- **R&D strategy**: devt of upstream and downstream parts of chain until ready to combine (FSBB chip)
  - upstream part (MIMOSA-22 and AROM chips) : CS + AC + DI + SC (part)
  - downstream part (SUZE chips) : ZS + OB + DT + SC (part)

\[\leftarrow \text{MIMO/AROM} \oplus \text{SUZE} (128\ \text{col.}) \rightarrow \text{FSBB-M/A} (448\ \text{col.}?) \rightarrow \text{MISTRAL/ASTRAL} (1344\ \text{col.}?)\]

- **Sensor specific to outer layers not yet included in devt plans ...**
Lessons from 2012

**Steps Validated:**
- Several in-pixel amplifiers lead to acceptable SNR & det. efficiency ($20 \times 20 \mu m^2$)
- $20 \times 33 \mu m^2$ pixels without in-pixel ampli. validated
- End-of-col. discriminators functionnal (noisy ?)

**Necessary Improvements:**
- Pixel circuitry noise: tail due few noisy pixels
  - → seems due to RTS noise
  - ⇒ requires optimising T geometries
- Pixel geometry and sensing system for rectangular pixels
**Engineering Run Submission**

- **CHIPS SUBMITTED:**
  - **Read-out architecture:**
    - pixel array: MIMOSA-22THRa (1 row), MIMOSA-22THRb (2 rows)
    - sparse data scan: SUZE-02
  - **In-pixel circuitry:**
    - noise mitigation: MIMOSA-32N1/N2
    - performance optimisation: MIMOSA-32FEE
    - charge sensing dependence on pixel dimensions & diode parameters: MIMOSA-34
  - **In-pixel charge encoding:** AROM-0 (1 bit), MIMADC (3 bits)

- **TESTS IN 2013:**
  - **Before TDR delivery:** only 2 months for testing ⇒ "comproimisation" of parallelised & most essential tests
  - **Plans:** all tests will be partial, in particular w.r.t. radiation tolerance (which should not be an issue)
    - Read-out architecture: validate rolling shutter on beam and 2-row read-out & sparse data scan in lab
    - In-pixel circuitry: demonstrate noise reduction in lab and improved pixel performance partially on beam
    - In-pixel charge encoding: validate in-pixel discriminator functioning at nominal speed in lab
Read-Out Architecture Developments

- **MIMOSA-22THRa : SINGLE-ROW READ-OUT**
  - Goal: validate architecture of full chain from charge collection to signal discrimination (translation of STAR-PXL chip)
  - 136 col. of 320 pixels ($22 \times 33 \, \mu m^2$) & 128 discri. 
  - 2 chips: 1 with pixel P-25 (M32ter) and 1 with P-26 (M32ter)
  - Test plan:
    - **TDR**: beam tests of part of 1 chip ($\epsilon_{det}$, fake, $\sigma_{SP}$) & lab tests of both chips ($\leq 7$ pixels) w/o some RL
    - **FSBB**: lab test of 7 pixels of both chips vs T, RL $\Rightarrow$ discri. threshold scan (FPN), pixel characterisation

- **MIMOSA-22THRb : DOUBLE-ROW READ-OUT**
  - Goal: validate double-row read-out approach
  - architecture derived from MIMOSA-22THRa, replacing single-row with double-row rolling shutter read-out (bottom sequencer)
  - 2 chips: 1 from IPHC, 1 from Irfu
  - 64 col. of 128 pixels ($22 \times 33 \, \mu m^2$) & 120 discri.
  - Test plan (lab exclusively):
    - **TDR**: demonstrate functionning at nominal frequency
    - **FSBB**: investigate performances vs freq., T, RL $\Rightarrow$ discri. threshold scan (FPN)
Data Sparsification and In-Pixel Digitisation

- **SUZE-02: SPARSIFICATION CIRCUITRY**
  - Goal: validate data compression architecture with L0 input (2D translation of STAR-PXL sparsification circuitry)
  - Test plan (lab essentially):
    - **TDR:** demonstrate architecture complies with design goals for most frequent patterns
    - **FSBB:** demonstrate archi. complies with all patterns & test SEE sensitivity (output buffers)

- **AROM-0: IN-PIXEL DISCRIMINATION**
  - Goal: compare 3 different high-precision in-pixel discriminators
  - Test plan (lab only):
    - **TDR:** demonstrate functionnality of at least 1 discr. variant
    - **AROM-1:** assess noise & threshold uniformity perfo. of the 3 diff. discr.

- **MIMADC: IN-PIXEL ADC**
  - Goal: compare 3 different (ramp, SAR) in-pixel 3-bit ADCs
  - Test plans (lab only):
    - **TDR:** no specific objective
    - **Q1/2014:** assess N, LSB, pixel-to-pixel dispersion of each ADC variant
**Investigation & Optimisation Chips**

- **MIMOSA-32FEE : IN-PIXEL AMPLIFICATION & CDS**
  - Goal : optimise in-pixel circuitry
  - Test plans (lab only) :
    - **TDR**: assess N, G, CCE perfo. for a few pixels (with RL ?)
    - Q1/2014: assess N, G, CCE perfo. for all 32 pixels vs T & RL
      → derive improved pixel design for FSBB

- **MIMOSA-32N : IN-PIXEL NOISE INVESTIGATION**
  - Goal: identify (mainly RTS like) noise sources and mitigate
  - 2 chips: 1 with sensing nodes, 1 without sensing nodes
  - Test plans (lab only) :
    - **TDR**: show solution to N distribution tail
    - Q1/2014: study all 32 pixels vs T & RL
      → derive improved pixel design for FSBB

- **MIMOSA-34 : CHARGE COLLECTION OPTIMISATION**
  - Goal : understand influence of sensing node parameters on charge coll.
    and optimise SNR for various pixel dimensions (inner & outer layers)
  - Test plans :
    - **TDR**: find optimal pixel dim. & sensing syst. (some beam tests + CCE&N in lab)
      → detection performance of a few pixels on beam (T, RL ?)
    - Q1/2014: study all 30 pixels and derive improved pixel design for FSBB
ASTRAL vs MISTRAL

- **ASTRAL vs MISTRAL**: Inner and Outer layer options

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Inner layers</th>
<th>Outer layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASTRAL</td>
<td>$15 \mu s \lesssim 150 \text{ mW/cm}^2$</td>
<td>$&lt; 30 \mu s \lesssim 70 \text{ mW/cm}^2$</td>
</tr>
<tr>
<td>MISTRAL</td>
<td>$30 \mu s &lt; 350 \text{ mW/cm}^2$</td>
<td>$&lt; 60 \mu s &lt; 180 \text{ mW/cm}^2$</td>
</tr>
</tbody>
</table>

- ASTRAL offers best performing architecture with particularly low power perspectives for outer layers ($\lesssim 70 \text{ mW/cm}^2$)
- Delay w.r.t. MISTRAL: in-pixel circuitry with discriminators not yet validated
- But global chip optimisation faster with ASTRAL (digital signals)
- Decision between FSBB-A & -M to be taken in Sept.-Oct. 2013 (input expected from Y. Degerli ?)

- **ACCELERATE ASTRAL DESIGN (≡ AROM) DESIGN**: AROM-1
  - Submission towards August ’13 (chips of $4 \times 4.5 \text{ mm}^2$)
  - $\geq 4$ alternative designs extending AROM-0 (Q1/13 engineering run)
    - Investigate analog-digital parasitic coupling on large surface
    - Different optimisations w.r.t. AROM-0 test results (2 chips)
    - Regulators vs distribution of threshold across pixel array (2 chips)
**Optimisation of Sparsification Parameters**

- **4 BASIC PARAM. PER SUZE-02 CIRCUIT (FSBB):**
  - Stage 1: up to 6 windows of $4 \times 5$ pixels selected per group of 32 columns
  - Stage 2: up to 12 windows selected per group of $\sim 200$ columns
  - Stage 3: up to 19 windows selected per FSBB ($\equiv 400$ columns)

- **LOGIC VALIDATED (SERGEY) WITH SIMUL. SETS OF 3 COLL. PILED UP ($\geq 1$ CENTRAL):**
  - Stage 1
  - Stage 2
  - Stage 3
Presently (almost) Uncovered Topics

• **CHIP DESIGN:**
  ✤ Use of trigger: added value not yet assessed (depends on integration time, occupancy → layer)
  ✤ Clock & voltage distribution schemes: to be validated with full chip
  ✤ Protection against SEU effects (sparsification circuitry, buffers, etc.): to assess with FSBB
  ✤ Etc.

• **OVERALL SYSTEM DESIGN:** Most crucial part of chips to address in the near future
  ✤ Signal transmission with embedded clock (8b10b not adapted to inner layers)
  ✤ Signal transmission drivers: proto. driver (M-32ter run) tested up to 1.5/2 GHz with ≲ 12 mW consumption (tbc)
  ✤ Multi-voltage standards to minimise power consumption
  ✤ Etc.

• **OUTER LAYER SENSOR DESIGN:** Extension of ASTRAL?
2014-16 Work Plan

- **Assumed status at end of 2013:**
  - Pixel designs optimised
  - Pixel array read-out architectures validated
  - Sparsification architecture almost fully validated
  - AROM-1 design(s) assessed
  - Decision taken to develop FSBB-A

- 2014: FSBB-A design(s) → submission Oct. 2014

- 2015: ASTRAL-0 design → submission Oct. 2015 (?)

- 2016: ASTRAL-1 design → submission Easter 2016 ?

- NB: If FSBB-M chosen in 2013 → final proto. submission likely < 2016
SUMMARY

- Expect Q1/13 engineering run to validate all main components of FSBB architecture

- Hope that AROM-0 tests (confirmed later by AROM-1) allow deciding for FSBB-A in Sept.-Oct. 2013 (using trigger ?)

- FSBB-A expected to be submitted in Oct. 2014 → ASTRAL-0 submitted in Oct. 2015

- Several pending aspects not (fully) covered at IPHC :
  ✴ SEE tolerance (e.g. output buffers)
  ✴ Signal transmission (driver) with embedded clock (optimisation)
  ✴ Voltage optimisation in digital circuitry
  ✴ Outer layer sensors
  ✴ Etc.
**Reticule Implantation Scheme**

- **Réticule ITS1 constitué de 26 circuits**

<table>
<thead>
<tr>
<th>Qty</th>
<th>Total Area mm$^2$</th>
<th>Area Ratio %</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPHC/IRFU</td>
<td>16</td>
<td>296,15</td>
</tr>
<tr>
<td>CERN</td>
<td>7</td>
<td>297,03</td>
</tr>
<tr>
<td>INESS</td>
<td>1</td>
<td>4,95</td>
</tr>
<tr>
<td>IPNL</td>
<td>1</td>
<td>1,08</td>
</tr>
<tr>
<td>RAL</td>
<td>1</td>
<td>47,29</td>
</tr>
</tbody>
</table>

- **Utilisation de la surface**

<table>
<thead>
<tr>
<th>Area mm$^2$</th>
<th>Ratio %</th>
<th>Value $</th>
<th>Value €</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reticule Area</td>
<td>666,50</td>
<td>100</td>
<td>381 000 285 750</td>
</tr>
<tr>
<td>Chip Area</td>
<td>646,51</td>
<td>97</td>
<td>369 570 277 178</td>
</tr>
<tr>
<td>Scribe Area</td>
<td>17,86</td>
<td>2,7</td>
<td>10 210 7 657</td>
</tr>
<tr>
<td>Min Width (100μm)</td>
<td>664,37</td>
<td>99,7</td>
<td>379 780 284 835</td>
</tr>
<tr>
<td>Effective Area</td>
<td>2,13</td>
<td>0,3</td>
<td>1 220 915</td>
</tr>
<tr>
<td>Wasted Area</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**430€ / mm$^2$ pour ce run**

---

CC - IPHC / PICSEL - 13/03/2013