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  - CBM-MVD
  - ILC
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- Summary & Outlook

SOURCES: Talks at CPIX-14 + VERTEX-14/15 + FEE-14 + TWEPP-13/14/15 + LHCC/ALICE + VCI-2016
SLIDES: M.Deveaux, D. Doehring, L.Greiner, Ch.Hu-Guo, M.Keil, M.Mager, L.Musa, F.Morel, F.Reidt, W.Snoeys, G. Aglieri, ...
Origin of CMOS Pixel Sensors

- **CMOS Pixel Sensors are derived from ASICS**
  - **Application-Specific Integrated Circuits**
  - ASICs populate every day's life: e.g. credit cards, PC, cell-phones, cars, washing machines, ...
  - industrial mass production item
    - (world revenue ~ several 100 billions USD/year)
  - key element: MOSFET transistors & conductive traces
    - printed in **Silicon** (usually)

- **C.M.O.S.**
  - **Complementary Metal Oxyde Semi-conductor**
    - widespread technology for constructing integrated circuits
      - used in microprocessors, microcontrollers, memories, etc.
• CMOS fabrication mode:
  ✴ \( \mu \)circuit lithography on a substrate sliced from a crystal ingot (or boule)
  ✴ proceeds through reticules (e.g. 21x23 or 25x32 mm\(^2\)) organised in wafers
CMOS Pixel Sensors: Main Features

- **Prominent features of CMOS pixel sensors:**
  - high granularity ⇒ excellent (micronic) spatial resolution
  - signal generated in (very) thin (15-40 μm) epitaxial layer
    → resistivity may be ≫ 1 kΩ · cm
  - signal processing μ-circuits integrated on sensor substrate
    ⇒ impact on downstream electronics and syst. integration (⇒ cost)

- **CMOS pixel sensor technology has the highest potential:**
  ⇒ R&D largely consists in trying to exploit potential at best
    with accessible industrial processes
  → manufacturing param. not optimised for particle detection:
    wafer/EPI characteristics, feature size, N(ML), ...

- **Read-out architectures:**
  - 1st generation: rolling shutter (synchronous) with analog pixel output (end-of-column discrim.)
  - 2nd generation: rolling shutter (synchronous) with in-pixel discrimination
  - 3rd generation: data driven (asynchronous) with in-pixel discrimination
  - ...

Twin-Well

Quadruple-Well
Role of the Epitaxial Layer

- **Main influences:**
  - $Q_{signal} \sim$ EPI thickness and doping profile
  - $\epsilon_{det}$ depends on depletion depth vs EPI thickness
  - NI radiation tolerance depends on depletion depth vs EPI thickness
  - Cluster multiplicity and $\sigma_{sp}$ depend on pixel pitch / EPI thickness

- **Case dependent optimisation mandatory:**
  - Deep depletion $\Rightarrow$ higher SNR (seed pixel) $\Rightarrow$ improved $\epsilon_{det}$ but degraded spatial resolution ....
  - Spatial resolution depends on Nb of bits encoding charge vs pixel pitch ...
  - Density of in-pixel circuitry depends on CMOS process options: feature size, Nb(ML), twin/quadruple-well, ...

![Diagrams showing approximate depletion depth, Epi-layer, drift time, and electric potential with EPI thicknesses of 18 \mu m and 25 \mu m.](image_url)
Main Components of the Signal Processing Chain

Typical components of read-out chain:
- AMP: In-pixel low noise pre-amplifier
- Filter: In-pixel filter
- ADC: Analog-to-Digital Conversion: 1-bit discriminator
  → may be implemented at column or pixel level
- Zero suppression: Only hit pixel information is retained and transferred
  → implemented at sensor periphery (usual) or inside pixel array
- Data transmission: O(Gbits/s) link implemented on sensor periphery

Read-Out alternatives:
- Synchronous: rolling shutter architecture
- Asynchronous: data driven architecture

Rolling shutter: best approach for twin-well processes
→ trade-off between performance, design complexity, pixel dimensions, power, ...
  → MIMOSA-26 (EUDET), MIMOSA-28 (STAR), ...
Overall Functionnality Distribution: Example of MIMOSA-26

CMOS 0.35 \( \mu \text{m} \) OPTO technology
Chip size: 13.7 x 21.5 mm\(^2\)

- Pixel array: 576 x 1152, pitch: 18.4 \( \mu \text{m} \)
- Active area: \(~10.6 \times 21.2\) mm\(^2\)
- In each pixel:
  - Amplification
  - CDS (Correlated Double Sampling)

Testability: several test points implemented all along readout path
- Pixels out (analogue)
- Discriminators
- Zero suppression
- Data transmission

Row sequencer
- Width: \(~350\) \( \mu \text{m} \)

1152 column-level discriminators
- Offset compensated high gain preamplifier followed by latch

Zero suppression logic

Reference Voltages Buffering for 1152 discriminators

I/O Pads
- Power supply Pads
- Circuit control Pads
- LVDS Tx & Rx

Current Ref.
- Bias DACs

Readout controller
- JTAG controller

Memory management
- Memory IP blocks

PLL, 8b/10b optional
Motivation for Developing CMOS Sensors

- CPS development triggered by need of very high granularity & low material budget

- Applications exhibit much milder running conditions than pp/LHC
  ⇒ Relaxed speed & radiation tolerance specifications

- Increasing panel of existing, foreseen or potential application domains:
  - Heavy Ion Collisions: STAR-PXL, ALICE-ITS, CBM-MVD, NA61, ...
  - $e^+e^-$ collisions: ILC, BES-3, ...
  - Non-collider experiments: FIRST, NA63, Mu3e, PANDA, ...
  - High precision beam telescopes adapted to medium/low energy electron beams:
    ➔ few $\mu m$ resolution achievable on DUT with EUDET-BT (DESY), BTF-BT (Frascati), ...
Several parameters govern the spatial resolution:

- **pixel pitch**
- epitaxial layer thickness and resistivity
- sensing node geometry & electrical properties
- cluster charge sharing between pixels
- signal encoding resolution

\[ \sigma_{sp} \text{ fct of pitch } \bigoplus \text{ SNR } \bigoplus \text{ charge sharing } \bigoplus \text{ ADCu, ...} \]

**Impact of pixel pitch (analog output):**

\[ \sigma_{sp} \sim 1 \text{ \( \mu \)m} \ (10 \text{ \( \mu \)m pitch}) \rightarrow \lesssim 3 \text{ \( \mu \)m} \ (40 \text{ \( \mu \)m pitch}) \]

**Impact of charge encoding resolution:**

- ex. of 20 \( \mu \)m pitch \[ \sigma_{sp}^{\text{digi}} = \text{pitch}/\sqrt{12} \sim 5.7 \text{ \( \mu \)m} \]

<table>
<thead>
<tr>
<th>Nb of bits</th>
<th>12</th>
<th>3-4</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>measured</td>
<td>reprocessed</td>
<td>measured</td>
</tr>
<tr>
<td>( \sigma_{sp} )</td>
<td>( \lesssim 1.5 \text{( \mu )m} )</td>
<td>( \lesssim 2 \text{( \mu )m} )</td>
<td>( \lesssim 3.5 \text{( \mu )m} )</td>
</tr>
</tbody>
</table>
State-of-the-Art: STAR-PXL

The STAR detector

@ RHIC

Method: Resolve displaced vertices (~120 µm)

200 GeV Au+Au collisions @ RHIC

\[ dN_{ch}/d\eta \sim 0.700 \text{ in central events} \]

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Quark Matter 2015 - Kobe, Japan
State-of-the-Art: STAR-PXL

Data taking from March-June 2014
State-of-the-Art: STAR-PXL

Data taking from March-June 2014

Validation of CPS for HEP (25/09/14: DoE final approval, based on vertexing performance assessment)

Preliminary courtesy of STAR collaboration
State-of-the-Art: STAR-PXL

Full validation of CPS for HEP (3 years physics program completed: 2014/15/16)

\[ R_{AA} = \frac{dN_{AA}/d\eta}{N_{\text{binary}} \cdot dN_{pp}/d\eta} \]

Data-taking from March-June 2014

\[ Au+Au \rightarrow D^0 @ 200 \text{ GeV} \ 0-10\% \]

\[ p_T (\text{GeV/c}) \]

\[ R_{AA} \]

\[ \pi 0-12\% \text{ STAR} \]

\[ p+ p \text{ uncert.} \]
Forthcoming Device: New ALICE Inner Tracking System

Upgrade of ALICE-ITS at LHC

7 layers, $> 10 \text{ m}^2$ active area with $\gg 10^4$ CPS

$\sigma_{sp} \lesssim 5 \mu m$

$\simeq 0.3 \% X_0 / \text{ layer}$
**CMOS Process Transition**: STAR-PXL $\rightarrow$ ALICE-ITS

- **Twin well process**: 0.6-0.35 $\mu$m
  - Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode
  - Limits choice of readout architecture strategy
  - Already demonstrate excellent performances
    - STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 $\mu$m process
      - $\epsilon_{\text{eff}} > 99.5\%$, $\sigma < 4$ $\mu$m
    - 1st CPS based VX detector at a collider experiment

- **Quadruple well process (deep P-well)**: 0.18 $\mu$m
  - N-well used to host PMOS transistors is shielded by deep P-well
  - Both types of transistors can be used
  - Widens choice of readout architecture strategies
    - Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18 $\mu$m process (quadruple well)
      - Synchronous Readout R&D:
        - proven architecture = safety
      - Asynchronous Readout R&D: challenging
### ITS Pixel Sensor: Two Architectures

#### Pixel Dimensions

- **ALPIDE:**
  - Pixel dimensions: $27\mu m \times 29\mu m$
  - Event time resolution: $5–10\ \mu s$
  - Power consumption: $< 50\text{mW/cm}^2$
  - Insensitive area: $\sim 1\text{mm} \times 30\text{mm}$

- **MISTRAL:**
  - Pixel dimensions: $36\mu m \times 65\mu m$
  - Event time resolution: $20\mu s$
  - Power consumption: $\sim 90\text{mW/cm}^2$
  - Insensitive area: $1.5\text{mm} \times 30\text{mm}$

#### Common Features

- Both chips have identical dim. (15mm x 30 mm) as well as physical and electrical interfaces:
  - position of interface pads
  - electrical signaling
  - steering, read-out, ... protocols

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Observed Detection Performances

- **FSBB-M & ALPIDE-2 beam tests**:
  - **FSBB-M**: No active epitaxy depletion
  - **ALPIDE**: Substrate reverse biased for the sake of SNR
Material budget: 0.05% $X_0$

Spatial resolution: $\sim 3-5 \mu m$

RADIATION TOLERANCE
How to improve speed & radiation tolerance while preserving 3-5 µm precision & < 0.1% X₀ ?

$O(10^2) \mu s$  

$O(10) \mu s$

$O(1) \mu s$

EUDET/STAR  
2010/14

ALICE/CBM  
2015/2019

?X?/ILC  
≥ 2020
Epitaxial Layer Depletion via Sensing Diode

- **Pegasus-2 sensor:**
  - Tower-Jazz 0.18 CIS process
  - 56 x 8 pixels (25 µm pitch)
  - Epitaxy: 18 µm, 1 kΩ · cm predominantly depleted
  - TN ≃ 16 ± 1 e⁻ ENC at 10°C
Looking into Future

- Stacked Multi-Layer CPS Devices:
  - **Charge particle tracker**
    - 3 points
    - Helix seed fit
    - Higher spatial resolution
    - Combined time & space res.
    - Higher Rad.Tol. by redundancy
    - 2-sided layers with 0.4 % X0 already exist from PLUME collaboration
  - **Multi-species detector**
    - Calorimeter
    - mixed W+Si sensors
    - Tracker
    - pure Si sensors
    - short e\_track indicates γ interaction
    - last fired layer indicates range
    - almost continuous track points for easy pattern recognition
    - 50 μm
    - Radio-emitters detection
    - Medical imaging
    - Nuclear physics
  - **X-ray spectro-imager**
    - Stacked
    - Higher counting dynamic
    - Higher QE @ high E
    - Location of point source detection
    - Energy spectrum from counting
    - Non destructive tests in Industry
    - Synchrotron instrumentation

- Self-determining CPS through integrated NN:
  - motivation: signal vs background discrimination, data compression
  - integrate NN used in image recognition
  - exploit VDSM CMOS processes’ trend towards smaller feature size
Monolithic CMOS Pixel Sensors are developed since 17 years for charged particle detection in subatomic physics.

They provide unprecedented detection and physics performances:
- Beam Telescopes providing precision tests on multi-GeV $\leftrightarrow$ sub-GeV $e^\pm$ beams (DESY, LNF)
- Vertex detectors providing unprecedented flavour tagging capabilities (STAR-PXL, FIRST)
- Various spin-offs

Their potential is far from being fully exploited:
- Their performances accompany the evolution of ASIC’s manufacturing industry, driven by a wide - and ever growing - spectrum of societal applications.
CONCLUSION and OUTLOOK

- Monolithic CMOS Pixel Sensors are developed since 17 years for charged particle detection in subatomic physics

- They provide unprecedented detection and physics performances:
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⇒ KIT-ADL HAS AN APPEALING FUTURE IN FRONT OF IT
Studies of 0.18 \( \mu m \) transistors exposed to TID \( \geq 10 \) MRad
- Measurements performed (+20\(^\circ\) C):
  - Leakage current & threshold shift
  - Increase of leakage current remains small
  - Threshold shifts remain small if \( W \gtrsim 2 \mu m \)
  - And are recoverable with thermal annealing

Studies of sensing node in 0.18 \( \mu m \) process at +20\(^\circ\) C:
- Pixel gain drops \( \geq 5 \) MRad (threshold shift ?)
  - But SNR seems acceptable up to 10 MRad
- Well known remedies seem efficient up to \( \gtrsim 10 \) MRad:
  - Short integration time, low temperature, ELT with guard rings
- Potential conflict: space available in high resolution pixels
Tolerance to Non-Ionising Radiation

- Main parameters governing the tolerance to NI radiation:
  - epitaxial layer: thickness and resistivity
  - sensing node: density, geometry, capacitance, depletion voltage
  - operating temperature
  - read-out integration time

- Most measurements performed with chips manufactured in two CMOS processes:
  - 0.35 µm with low & high resistivity epitaxy
  - 0.18 µm with high & resistivity epitaxy (mainly 18 & 20 µm thick)

- Clear improvement with 0.18 µm process w.r.t. 0.35 µm process
  - ALICE-ITS requirement seems fulfilled: 2.7 MRad & $1.7 \cdot 10^{13} n_{eq}/cm^2$ at $T = +30^\circ C$
  - Fluences in excess of $10^{14} n_{eq}/cm^2$ seem within reach
    \[\Rightarrow\text{ requires global optimisation of design & running parameters}\]
PIPHER-2 prototype

- Pixel pitch 22 um, collection diode diameter 5 um
- Measurements with 55Fe source, temperature ~15 °C
- Spectrum of 5.9 (6.4) keV mixed for 1024 individual pixels

- Saturation for epi 18um ⇒ full depletion
- Peak entries (CZ / epi-18) = 2 ⇒ depletion depth beyond 40 um
Motivation for High Precision CMOS Sensors