Development of CMOS Pixel Sensors for HIGH-PRECISION Vertexing & Tracking Devices

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Contents

- Primordial motivations & main features of CMOS sensors
- 1st architecture developed - state of the art
  - MIMOSA-26 (EUDET chip applications) $\rightarrow$ MIMOSA-28 (STAR-PXL)
- Extension towards more demanding experiments
  - ALICE-ITS & -MFT
  - CBM-MVD
  - ILC
- Perspectives & forthcoming challenges
  - read-out speed & rad. tolerance
  - architectures & emerging CMOS technologies
- Conclusion

SOURCES: Talks at CPIX-14 + VERTEX-14 + FEE-14 + TWEPP-13/14 + LHCC/ALICE
SLIDES: M.Deveaux, L.Greiner, Ch.Hu-Guo, M.Keil, M.Mager, L.Musa, F.Morel, D.Muenstermann, I.Peric, F.Reidt, W.Snoeys
Motivation for Developing CMOS Sensors

- CPS development triggered by need of very high granularity & low material budget
- Applications exhibit much milder running conditions than pp/LHC
  ⇒ Relax speed & radiation tolerance specifications
- Increasing panel of existing, foreseen or potential application domains:
  - Heavy Ion Collisions: STAR-PXL, ALICE-ITS, CBM-MVD, NA61, ...
  - $e^+e^-$ collisions: ILC, BES-3, ...
  - Non-collider experiments: FIRST, NA63, Mu3e, PANDA, ...
  - High precision beam telescopes adapted to medium/low energy electron beams:
    → few $\mu m$ resolution achievable on DUT with EUDET-BT (DESY), BTF-BT (Frascati), ...
Example of Application: ILC Vertex Detector

- **Goal:** $\sigma_{sp} \lesssim 3 \mu m$ in both directions with $\lesssim 0.15\% X_0 / \text{layer}$

- **Comparison:** $\sigma_{sp} = 3x3 \mu m^2$ & $0.15\% X_0$ against $14x70 \mu m^2$ & $1.0\% X_0$
Example of Application: Upgrade of ALICE-ITS

- ALICE Inner Tracking System (ITS) foreseen to be replaced during LS2/LHC
  - higher luminosity, improved charm tagging

- Expected improvement in pointing resolution and tracking efficiency
Long Term R&D

- R&D activity of CPS initiated in 1999 for future subatomic physics experiments
- First contact for STAR PXL took place in Year 2000 during the workshop Vertex-2000
Prominent features of CMOS pixel sensors:

- high granularity ⇒ excellent (micronic) spatial resolution
- signal generated in very thin (15-40 \( \mu m \)) epitaxial layer
  \( \overset{\leftarrow}{\Rightarrow} \) resistivity may be \( \gg 1 \text{k}\Omega \cdot \text{cm} \)
- signal processing \( \mu \)-circuits integrated on sensor substrate
  ⇒ impact on downstream electronics and syst. integration (⇒ cost)

CMOS pixel sensor technology has the highest potential:

⇒ R&D largely consists in trying to exploit potential at best
  with accessible industrial processes
  \( \overset{\leftarrow}{\Rightarrow} \) manufacturing param. not optimised for particle detection:
  wafer/EPI characteristics, feature size, N(ML), ...

Read-out architectures:

- 1st generation: rolling shutter (synchronous) with analog pixel output (end-of-column discrim.)
- 2nd generation: rolling shutter (synchronous) with in-pixel discrimination
- 3rd generation: data driven (asynchronous) with in-pixel discrimination
  ...

Twin-Well

Quadraple-Well
Measured Spatial Resolution

- Several parameters govern the spatial resolution:
  - pixel pitch
  - epitaxial layer thickness and resistivity
  - sensing node geometry & electrical properties
  - signal encoding resolution

  \[ \sigma_{sp} \text{ fct of pitch} \oplus \text{SNR} \oplus \text{charge sharing} \oplus \text{ADCu}, ... \]

- Impact of pixel pitch (analog output):
  \[ \sigma_{sp} \sim 1 \, \mu m \text{ (10 } \mu m \text{ pitch)} \leq 3 \, \mu m \text{ (40 } \mu m \text{ pitch)} \]

- Impact of charge encoding resolution:
  - ex. of 20 \( \mu m \) pitch \( \Rightarrow \sigma_{sp}^{\text{digi}} = \text{pitch}/\sqrt{12} \sim 5.7 \, \mu m \)

<table>
<thead>
<tr>
<th>Nb of bits</th>
<th>12</th>
<th>3-4</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>measured</td>
<td>reprocessed</td>
<td>measured</td>
</tr>
<tr>
<td>( \sigma_{sp} )</td>
<td>( \lesssim 1.5 \mu m )</td>
<td>( \lesssim 2 \mu m )</td>
<td>( \lesssim 3.5 \mu m )</td>
</tr>
</tbody>
</table>
Example of Application: Upgrade of ALICE-ITS

Typical components of read-out chain:

- **AMP**: In-pixel low noise pre-amplifier
- **Filter**: In-pixel filter
- **ADC**: Analog-to-Digital Conversion: 1-bit discriminator
  - may be implemented at column or pixel level
- **Zero suppression**: Only hit pixel information is retained and transferred
  - implemented at sensor periphery (usual) or inside pixel array
- **Data transmission**: O(Gbits/s) link implemented on sensor periphery

Read-Out alternatives:

- **Synchronous**: rolling shutter architecture
- **Asynchronous**: data driven architecture

Rolling shutter: best approach for twin-well processes

- trade-off between performance, design complexity, pixel dimensions, power, ...
- MIMOSA-26 (EUDET), MIMOSA-28 (STAR), ...
Main characteristics of MIMOSA-26 sensor equipping EUDET BT:

- 0.35 \( \mu m \) process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)
- Column architecture with in-pixel amplification (cDS) and end-of-column discrimination, followed by \( \varnothing \)
- Binary charge encoding
- Active area: 1152 columns of 576 pixels (21.2 \( \times \) 10.6 mm\(^2\))
- Pitch: 18.4 \( \mu m \) \( \rightarrow \) \( \sim \) 0.7 million pixels
  - Charge sharing \( \Rightarrow \) \( \sigma_{sp} \sim 3.\text{-}3.5 \mu m \)
- \( t_{r.o.} \leq 100 \mu s \) (\( \sim 10^4 \) frames/s)
  - Suited to \( \geq 10^6 \) part./cm\(^2\)/s
- JTAG programmable
- Rolling shutter architecture
  - Full sensitive area dissipation \( \cong 1 \) row
  - \( \Rightarrow \) \( \sim 250 \) mW/cm\(^2\) power consumption (fct of \( N_{col} \))
- Thinned to 50 \( \mu m \) (yield \( \sim 90\%\))

Various applications: VD demonstrators, NA63, NA61, FIRST, oncotherapy, dosimetry, ...
PXL in STAR Inner Detector Upgrades

TPC – Time Projection Chamber
(main tracking detector in STAR)

HFT – Heavy Flavor Tracker
- SSD – Silicon Strip Detector
  - $r = 22$ cm
- IST – Inner Silicon Tracker
  - $r = 14$ cm
- PXL – Pixel Detector
  - $r = 2.8, 8$ cm

Direct topological reconstruction of Charm – displaced vertices

We track inward from the TPC with graded resolution:

\[
\begin{align*}
\text{TPC} & \sim 1\text{mm} \\
\text{SSD} & \sim 300\mu\text{m} \\
\text{IST} & \sim 250\mu\text{m} \\
\text{PXL} & \sim 30\mu\text{m}
\end{align*}
\]
Main characteristics of ULTIMATE (≡ MIMOSA-28):

- 0.35 µm process with high-resistivity epitaxial layer
- column // architecture with in-pixel cDS & amplification
- end-of-column discrimination & binary charge encoding
- on-chip zero-suppression
- active area: 960 columns of 928 pixels (19.9 × 19.2 mm²)
- pitch: 20.7 µm → ~ 0.9 million pixels
  → charge sharing ⇒ σ_sp ≥ 3.5 µm
- JTAG programmable
- t_r.o. ≤ 200 µs (∼ 5 × 10³ frames/s) ⇒ suited to >10⁶ part./cm²/s
- 2 outputs at 160 MHz
- ≤ 150 mW/cm² power consumption

Sensors FULLY evaluated/validated: (50 µm thin)

- N ≤ 15 e⁻ ENC at 30-35°C
- ε_{det}, fake & σ_sp as expected
- Rad. tol. validated (3·10⁻¹² n_{eq}/cm² & 150 kRad at 30°C)
- All specifications were met ⇒ 2 detectors of 40 ladders constructed

1st physics data taking: March to June 2014 ⇒ measured σ_{ip}(p_T) match requirements
Validation of CPS for HEP (25/09/14: DoE final approval, based on vertexing performance assessment)
Preliminary Results of STAR-PXL Run: Hit multiplicity

- Hit pixel multiplicity per ladder ($\equiv$ 10 chips) and per layer (courtesy of STAR collaboration)

**[PXL] Number of Hits per Ladder**

- Nb(hit pixels / ladder)

**[PXL] Hit Correlation Inner-Outer Layer**

- Inner barrel sensors see $O(100)$ hits ($\equiv$ 4 pixels) per frame
Preliminary Results of STAR-PXL Run

- **Benchmark**: measured impact parametre resolution for 700-800 MeV/c kaons:
  - Figure (courtesy of STAR collaboration) displays resolutions on DCA in $R\Phi$ and $Z$
  - Data collected with low luminosity (clean TPC environment)
  - Tracks traversing the ladders equipped with Al traces
  - Results are still **PRELIMINARY**

$n \Rightarrow 40 \, \mu \text{m}$ obtained for 700-800 MeV/c kaons in both directions, as expected
Next Challenge: ALICE-ITS Upgrade

- Upgrade of ITS **entirely based on CPS**:
  - Present geometry: 6 layers
    - HPS x 2 / Si-drift x 2 / Si-strips x 2
  - Future geometry: 7 layers → → → all with CPS (∼ 25-30 · 10^3 chips)
    - 1st large tracker (10 m^2) using CPS
  - ITS-TDR approved March 2014:

- Requirements for ITS inner and outer barrels compared to specifications of STAR-PXL chip:

<table>
<thead>
<tr>
<th></th>
<th>(\sigma_{sp})</th>
<th>(t_{r.o.})</th>
<th>Dose</th>
<th>Fluency</th>
<th>(T_{op})</th>
<th>Power</th>
<th>Active area</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>&lt; 4 (\mu m)</td>
<td>&lt; 200 (\mu s)</td>
<td>150 kRad</td>
<td>(3 \cdot 10^{12} n_{eq}/cm^2)</td>
<td>30-35°C</td>
<td>160 mW/cm^2</td>
<td>0.15 m^2</td>
</tr>
<tr>
<td>ITS-in</td>
<td>&lt; 5 (\mu m)</td>
<td>&lt; (30 \mu s)</td>
<td>700 kRad</td>
<td>(1 \cdot 10^{13} n_{eq}/cm^2)</td>
<td>30°C</td>
<td>&lt; 300 mW/cm^2</td>
<td>0.17 m^2</td>
</tr>
<tr>
<td>ITS-out</td>
<td>&lt; 10 (\mu m)</td>
<td>&lt; (30 \mu s)</td>
<td>15 kRad</td>
<td>(4 \cdot 10^{11} n_{eq}/cm^2)</td>
<td>30°C</td>
<td>&lt; 100 mW/cm^2</td>
<td>(\sim 10 m^2)</td>
</tr>
</tbody>
</table>

⇒ 0.35 \(\mu m\) CMOS process (STAR-PXL) marginally suited to read-out speed & radiation tol.
**CMOS Process Transition: STAR-PXL ↔ ALICE-ITS**

- **Twin well process: 0.6-0.35 μm**
  - Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode
  - Limits choice of readout architecture strategy
  - Already demonstrate excellent performances
    - STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 μm process
      - $\epsilon_{\text{eff}} > 99.5\%$, $\sigma < 4 \mu\text{m}$
    - 1st CPS based VX detector at a collider experiment

- **Quadruple well process (deep P-well): 0.18 μm**
  - N-well used to host PMOS transistors is shielded by deep P-well
  - Both types of transistors can be used
  - Widens choice of readout architecture strategies
    - Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18 μm process (quadruple well)
      - Synchronous Readout R&D:
        - proven architecture = safety
      - Asynchronous Readout R&D: challenging
Sensing Node & VFEE Optimisation

- **General remarks on sensing diode:**
  - should be small because: $V_{signal} = \frac{Q_{coll}}{C}$; Noise $\sim C$; $G_{PA} \sim \frac{1}{C}$
  - BUT should not be too small since $Q_{coll} \sim CCE$ (important against NI irradiation)

- **General remarks on pre-amplifier** connected to sensing diode:
  - should offer high enough gain to mitigate downstream noise contributions
  - should feature input transistor with minimal noise (incl. RTS)
  - should be very close to sensing diode (minimise line C)

- **General remarks on depletion voltage:**
  - apply highest possible voltage on sensing diode
    - preserving charge sharing $\leftrightarrow \sigma_{sp}$
  - alternative: backside/reverse biasing

$\Rightarrow$ **Multiparametric trade-off to be found,**
based on exploratory prototypes rather than on simulations
Charge Sensing Element $\rightarrow$ Optimal SNR

- **Influence of sensing diode area**
  - Sensing diode cross-section varied from $10.9 \, \mu m^2$ to $8 \, \mu m^2$ underneath $10.9 \, \mu m^2$ large footprint
  - Suppresses low SNR tail $\rightarrow$ enhances detection efficiency (and mitigates effect of fake rate)

- **Benefit from reducing the sensing diode area**
ITS Pixel Chip – two architectures

ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

L. Musa
(LHCC 03/03/15)

(*) might further reduce to 73mW/cm²
Synchronous Read-Out Architecture: Rolling Shutter Mode

- **Design addresses 3 issues:**
  - Increasing S/N at pixel-level
  - A to D Conversion: at column-level (MISTRAL) at pixel-level (ASTRAL)
  - Zero suppression (SUZE) at chip edge level

![Diagram of Pixel Array and Window of 4x5 pixels]

- **Power vs speed:**
  - **Power:** only the selected rows (N=1, 2, ...) to be read out
  - **Speed:** N rows of pixels are read out in //
  - **Integration time = frame readout time**
    \[
    t_{\text{int}} = \frac{(\text{Row readout time}) \times (\text{No. of Rows})}{N}
    \]
Detection Performances of MISTRAL Building Block

- $\epsilon_{det}$, fake rate, $\sigma_{res}$ vs Discriminator Threshold: Noise averaged over 11 thinned sensors

- MISTRAL-O composed of 3-4 identical Full Scale Building Blocks operated in parallel & multiplexed at their outputs (prototype pixel dim. : 22 x 33 $\mu m^2$)

- Beam tests with a few GeV electrons (DESY)
  - Valid threshold range $\sim 7$–$12$ TN ($T = 30^\circ C$)
    - $\epsilon_{det} > 99\%$ and $\sigma_{sp} \lesssim 5 \mu m$
    - Fake rate ($\equiv$ noise fluctuations) $< 10^{-5}$
Asynchronous Read-Out Architecture: ALPIDE (Alice Pixel DETector)

- Design concept similar to hybrid pixel read-out architecture exploiting availability of TJsc CIS quadruple well process: pixel hosts N- & P-MOS transistors

- Each pixel features a continuously power active
  - low power consuming analogue front end ($P < 50$ nW/pixel)
    - based on a single stage amplifier with shaping / current comparator
      - amplification gain $\sim 100$
      - shaping time $\sim$ few $\mu$s
  - Data driven read-out of the pixel matrix
    $\Rightarrow$ only zero-suppressed data are transferred to periphery
Asynchronous Read-Out Architecture: ALPIDE

- Low power in-pixel discriminator
- Current comparator (bias of ~20 nA)
- Storage element for hit information

- In-matrix address encoder
- Tree structure to decrease capacitive load of lines
- Outputs pixel address and resets pixel storage element

- Loss-less data compression de-randomizing circuit
- Compresses cluster information in the column
- Multi-event memory
ALPIDE Detection Performance Assessment

- ALPIDE-1 beam tests (5–7 GeV pions):
  - Final sensor dimensions: 15 mm × 30 mm
  - About 0.5 M pixels of 28 µm × 28 µm
  - 4 different sensing node geometries
  - Possibility of reverse biasing the substrate
    → default: -3 V
  - Possibility to mask pixels (fake rate mitigation)
    → default: O(10^{-3}) masked pixels

![Image of ALPIDE sensor](image.png)

![Graphs showing efficiency, noise occupancy per pixel, and resolution](graphs.png)
• Studies of 0.18 $\mu$m transistors exposed to TID $\geq$ 10 MRad
  - measurements performed (+20°C):
    - leakage current & threshold shift
  - increase of leakage current remains small
  - threshold shifts remain small if $W \geq 2\mu$m
    and are recoverable with thermal annealing

• Studies of sensing node in 0.18 $\mu$m process at +20°C:
  - Pixel gain drops $> 5$ MRad (threshold shift ?)
    - but SNR seems acceptable up to 10 MRad
  - Well known remedies seem efficient up to $\gtrsim 10$ MRad:
    - short integration time, low temperature, ELT with guard rings
  - Potential pb: space available in high resolution pixels
Tolerance to Non-Ionising Radiation

- **Main parameters governing the tolerance to NI radiation:**
  - epitaxial layer: thickness and resistivity
  - sensing node: density, geometry, capacitance, depletion voltage
  - operating temperature
  - read-out integration time

- **Most measurements performed with chips manufactured in two CMOS processes:**
  - 0.35 µm with low & high resistivity epitaxy
  - 0.18 µm with high & resistivity epitaxy (mainly 18 & 20 µm thick)

- **Clear improvement with 0.18 µm process w.r.t. 0.35 µm process**
  - ALICE-ITS requirement seems fulfilled: 700 kRad & $10^{13} \text{n}_{eq}/\text{cm}^2$ at $T = +30^\circ \text{C}$
  - Fluences in excess of $10^{14} \text{n}_{eq}/\text{cm}^2$ seem within reach
    $\Rightarrow$ requires global optimisation of design & running parameters
Forthcoming Challenges

How to reach the bottom right corner of the "Quadrature"?
Improving Speed and Radiation Tolerance

How to improve speed & radiation tolerance while preserving 3-5\(\mu\)m precision & < 0.1\% \(X_0\)?
Further Perspectives of Performance Improvement

- **Expected added value of HV-CMOS:**
  - Benefits from extended sensitive volume depletion:
    - faster charge collection
    - higher radiation tolerance
  - Not bound to CMOS processes using epitaxial wafers
    ⇒ easier access to VDSM (< 100 nm) processes
    ⇒ higher in-pixel micro-circuit density

- **Questions:**
  - minimal pixel dimensions vs $\sigma_{sp} \lesssim 3 \mu m$?
  - uniformity of large pixel array, yield?

- **Attractive possible evolution: 2-tier chips**
  - signal sensing & processing functionality distributed over 2 tiers interconnected at pixel level (capa. coupling)
  - combine 2 different CMOS processes if advantageous:
    1 optimal for sensing, 1 optimal for signal processing
  - benefit: small pixel $\rightarrow$ resolution, fast response,
    data compression, robustness?
  - challenge: interconnection technology (reliability, cost, ...)

Ivan Peric: CPIX14, Bonn, 2014
CONCLUSION

- CPS have demonstrated that they can provide the spatial resolution and material budget required for numerous applications

- CPS are suited for vertex detectors ($\ll 1 \text{ m}^2$)
  \[\rightarrow\text{ attractive features for tracking devices (} \gg 1 \text{ m}^2\text{), incl. cost (!)}\]

- Forthcoming & Upcoming challenges:
  - Large active area: ALICE-ITS $\equiv 10 \text{ m}^2$ to cover with 20-30,000 sensors
  - Radiation tolerance: $\gtrsim 10 \text{ MRad} \& \gtrsim 10^{14} \text{ n}_{eq}/\text{cm}^2$ (e.g. CBM at SIS-300)
  - Read-out speed: $\lesssim 1 \mu\text{s}$ (e.g. ILC vertex detector & tracker)

- Perspectives:
  - HV-CPS but exposed to challenges if small pixels and very low power consumption are required
    \[\rightarrow\text{ VDSM processes ?}\]
  - 2-tier sensors $\equiv$ (sensing + ampli) $\oplus$ (sparsification + data transfer)
    combining 2 CMOS processes at pixel level
    \[\rightarrow\text{ still an R&D ...}\]
CMOS Pixel Sensors (CPS): A Long Term R&D

- **Ultimate objective: ILC, with staged performances**
  - CPS applied to other experiments with intermediate requirements

**EUDET 2006/2010**
Beam Telescope

**EUDET (R&D for ILC, EU project)**
**STAR (Heavy Ion physics)**
**CBM (Heavy Ion physics)**
**ILC (Particle physics)**
**HadronPhysics2 (generic R&D, EU project)**
**AIDA (generic R&D, EU project)**
**FIRST (Hadron therapy)**
**ALICE/LHC (Heavy Ion physics)**
**EIC (Hadron physics)**
**CLIC (Particle physics)**
**BESIII (Particle physics)**

**ALICE 2018**
A Large Ion Collider Experiment

**CBM >2018**
Compressed Baryonic Matter

**STAR 2013**
Solenoidal Tracker at RHIC

**ILC >2020**
International Linear Collider
**Influence of sensing diode area**

- Optimum sensing diode geometry between
  - the smallest for the sake of $C$, $N$, $G_{PA}$
  - but not too small to preserve CCE (rad. tol.)
- 10.9 $\mu m^2$ large sensing diode
- 8 $\mu m^2$ cross-section sensing diode
  - underneath 10.9 $\mu m^2$ large footprint

  $\Rightarrow$ Improves SNR $\Rightarrow$ Detection efficiency
Large Pixels for Outer Layers?

- **Motivation for LARGE pixels**: reduced power (& read-out time) in case of alleviated spatial resolution requirement
  \[ \Rightarrow \text{adequate for L3-6 (also required rad. tol. alleviated)} \]

\[
\begin{array}{|c|c|c|}
\hline
\text{MIMOSA 34, Pixel 22x66 \(\mu\text{m}^2\), diode 15 \(\mu\text{m}\)} & \text{Estimated efficiency} & \text{MIMOSA 34, binary emulation, cluster multiplicity} \\
\hline
\text{epi. 20 \(\mu\text{m}\)} & \text{hSNReal} & \text{epi. HR 20 \(\mu\text{m}\) at } T_{\text{cool}}=30\degree\text{C} \\
\hline
\text{Entries} & 2031 & \text{pixel 22x33 \(\mu\text{m}^2\), diode 11 \(\mu\text{m}\)} \\
\text{Mean} & 60.6 & \text{pixel 22x66 \(\mu\text{m}^2\), diode 15 \(\mu\text{m}\)} \\
\text{RMS} & 30.37 & \\
\chi^2 / \text{ndf} & 80.53 / 66 & \\
\text{Constant} & 353 \pm 12.0 & \\
\text{MPV} & 42.05 \pm 0.65 & \\
\text{Sigma} & 12.37 \pm 0.37 & \\
\hline
\end{array}
\]

- **Difficulty**: keep high CCE (all over the pixel) without substantial (capacitive) noise increase and gain loss

- **Results**: tests with 4.4 GeV electrons, no in-pixel CDS
  
  - SNR(MPV) \(\sim 42.1 \pm 0.7 \Rightarrow \epsilon_{\text{det}} \sim 100\%\)
  
  - cluster multiplicity \((22 \times 66) \sim \text{cluster multiplicity } (22 \times 33) \sim 3 \text{ (mean)}\)
**MISTRAL & ASTRAL**: Schematics & Layouts

- **MISTRAL**: rolling shutter with 2-row read-out & end-of column discriminators

- **ASTRAL**: rolling shutter with 2-row read-out (≡ MISTRAL) & in-pixel discriminators

- 1st Full Scale Building Blocks (FSBB) fab. in Spring ’14 ➔ FSBB-M0 tests ± completed
MISTRAL Architecture Validation

1st step: Separate validation of each element composing signal sensing & processing chain:
- Pixel array with 1-row read-out (1 discri./column)
- Pixel array with 2-row read-out (2 discri./column)
- Zero suppression circuitry with output buffers

2nd step: FSBB-M

\( \cong \frac{1}{3} \text{of MISTRAL:} \)

<table>
<thead>
<tr>
<th>threshold</th>
<th>fake rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 mV</td>
<td>11870</td>
</tr>
<tr>
<td>5 mV</td>
<td>3584</td>
</tr>
<tr>
<td>6 mV</td>
<td>1092</td>
</tr>
<tr>
<td>7 mV</td>
<td>406</td>
</tr>
<tr>
<td>8 mV</td>
<td>236</td>
</tr>
</tbody>
</table>

\( TN \cong 0.87 \text{mV} \quad \text{FPN} \cong 0.55 \text{mV} \quad (\text{total noise} \cong 20 \text{e}^{-} \text{ENC}) \)
**Synchronous Read-Out Architecture: In-Pixel Discrimination**

- To provide adequate performance within small pixel
  - Structure selection: speed & power & offset mitigation vs area
    - Diffential structure: preferable in mixed signal design
    - Two auto-zero amplifying stages + dynamic latch
      - OOS (Out Offset Storage) for the first stage and IOS (Input Offset Storage) for the second
  - Gain and power optimized amplifier
  - Very careful layout design to mitigate cross coupling effects
  - Conversion time: 100 ns; current: ~14 µA/discriminator

- Test results of in-pixel discriminator:
  - Discriminators alone: TN ~ 0.29 mV, FPN ~ 0.19 mV
  - Discriminators + FEE: TN ~ 0.94 mV, FPN ~ 0.23 mV
Asynchronous Read-Out Architecture: ALPIDE (Alice Pixel DEtector)

- Design concept similar to hybrid pixel readout architecture thanks to availability of Tower CIS quadruple well process: both N & P MOS can be used in a pixel

- Each pixel features a continuously power active:
  - Low power consumption analogue front end (Power < 50 nW/pixel) based on a single stage amplifier with shaping / current comparator
    - High gain ~100
    - Shaping time few μs
  - Dynamic Memory Cell, ~80 fF storage capacitor which is discharged by an NMOS controlled by the Front-End

- Data driven readout of the pixel matrix, only zero-suppressed data are transferred to the periphery

Courtesy of W. Snoeys / TWEPP-2013
Perspectives : 2-Tier HV-CPS

- **Attractive possible evolution : 2-tier chips**
  - signal sensing & processing functionalities distributed over 2 tiers interconnected at pixel level (capa. coupling)
  - combine 2 different CMOS processes if advantageous:
    - 1 optimal for sensing, 1 optimal for signal processing
  - benefit: small pixel → resolution, fast response, data compression, robustness?
  - challenge: interconnection technology (reliability, cost, ...)

- **On-going R&D : ATLAS upgrade for HL-LHC**
  - HV2FEI4 chip ≡ sensitive HV-CPS tier (180 nm process) interconnected to FEI4 ROC (130 nm process)
  - radiation tolerance test results encouraging, threshold dispersion?
  - promising perspective: high-resistivity EPI (≈ ALICE-ITS)

- **Other applications envisaged/foreseen :**
  - ATLAS strip like read-out  
  - CLIC vertex detector
  - Mu3e experiment: analog pixel read-out with remote signal processing circuitry
Boundaries of the CPS Development

- **New fabrication process**:
  - Expected to be radiation tolerant enough
  - Expected to allow for fast enough read-out
  - Larger reticule ($\lesssim 25 \text{ mm} \times 32 \text{ mm}$)

- **Drawbacks of smaller feature size**
  - $1.8 \text{ V}$ operating voltage (instead of $3.3 \text{ V}$)
    - $\Rightarrow$ reduced dynamics in signal processing circuitry and epitaxy depletion voltage
  - increased risk of Random Telegraph Signal (RTS) noise

- **Consequences of the large surface to cover**
  - good fabrication yield required $\Rightarrow$ sensor design robustness
  - mitigate noisy pixels (data transmission band width)
  - sensor operation should be stable along $1.5 \text{ m}$ ladder (voltage drop !)
  - minimal connections to outside world (material budget)
    - $\Rightarrow$ impacts sensor periphery (slow control, steering parameters, ...)

<table>
<thead>
<tr>
<th>STAR-PXL</th>
<th>ALICE-ITS</th>
<th>added-value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0.35 \mu m$</td>
<td>$0.18 \mu m$</td>
<td>speed, TID, power</td>
</tr>
<tr>
<td>4 ML</td>
<td>6 ML</td>
<td>speed, power</td>
</tr>
<tr>
<td>twin-well</td>
<td>quadruple-well</td>
<td>speed, power</td>
</tr>
<tr>
<td>EPI $14/20 \mu m$</td>
<td>EPI $18/40 \mu m$</td>
<td>SNR</td>
</tr>
<tr>
<td>EPI $\gtrsim 0.4 \Omega \cdot \text{cm}$</td>
<td>EPI $\sim 1 - 8 \Omega \cdot \text{cm}$</td>
<td>SNR, NITD</td>
</tr>
</tbody>
</table>
Sensing Node & VFEE Optimisation

- **General remarks on sensing diode:**
  - should be small because: \( V_{signal} = \frac{Q_{coll}}{C} \); Noise \( \sim C \); \( G_{PA} \sim \frac{1}{C} \)
  - BUT should not be too small since \( Q_{coll} \sim CCE \) (important against NI irradiation)

- **General remarks on pre-amplifier** connected to sensing diode:
  - should offer high enough gain to mitigate downstream noise contributions
  - should feature input transistor with minimal noise (incl. RTS)
  - should be very close to sensing diode (minimise line C)

- **General remarks on depletion voltage:**
  - apply highest possible voltage on sensing diode preserving charge sharing \( \leftrightarrow \sigma_{sp} \)
  - alternative: backside biasing

\( \Rightarrow \) **Multiparametric trade-off to be found, based on exploratory prototypes rather than on simulations**
Outcome of 2012 Exploration of the 0.18 $\mu m$ Process

- **Steps Validated in 2012:**
  - Several in-pixel amplifier variants lead to satisfactory SNR & det. eff. $(20 \times 20 \mu m^2)$ incl. after 1 MRad & $10^{13} n_{eq}/cm^2$ at $30^\circ C$
  - Results pres. at VCI-2013 (J. Baudot)

- **Call for Improvement:**
  - Pixel circuitry noise:
    - tail due few noisy pixels
    - attributed to RTS noise
    - required optimising T geometries

![Graphs and plots showing signal/noise ratios and histograms for different conditions.](image-url)
Established knowledge on radiation tolerance

Sensors cooled to -15°C

AMS 0.35

AMS 0.35 HR

T = -35°C

Radiation hardness \([n_{eq}/cm^2]\)

Effective pixel pitch [\(\mu m\)] := \(\sqrt{\text{Pixel surface}}\)

M. Deveaux, CPIX Workshop, Sept. 15th – 17th 2014, Bonn
Pixel Optimisation : Epitaxial Layer and Sensing Node

- **Pixel charge coll. perfo. for HR-18 & VHR-20 (no in-pixel CDS):**
  - SNR distributions $\leftrightarrow$ MPV & low values tail
  - $22 \times 33 \, \mu m^2$ (2T) pixels at $30^\circ C$

  $\Rightarrow$ **Results:**
  - only $\sim 0.1 \%$ of cluster seeds exhibit $SNR \lesssim 7–8$
  - $SNR(VHR-20) \sim 5-10\%$ higher than $SNR(HR-18)$

- **Pixel charge coll. perfo. for 2 diff. sensing nodes:**
  - $10.9 \, \mu m^2$ large sensing diode
  - $8 \, \mu m^2$ cross-section sensing diode
    - underneath $10.9 \, \mu m^2$ large footprint

  $\Rightarrow$ **Results:**
  - $8 \, \mu m^2$ diode features nearly 20% higher $SNR(MPV)$
    & much less pixels at small $SNR$ (e.g. $SNR < 10$)
    $\Rightarrow Q_{clus} \sim 1350/1500$ e$^-$ for $8/10.9 \, \mu m^2$
  - marginal charge loss with $8 \, \mu m^2$ diode
  - radiation tolerance to $250$ kRad & $2.5 \cdot 10^{12}$ n$_{eq}$/cm$^2$ at $30^\circ C$ OK
In-Pixel Pre-Amp & Clamping : SNR of Pixel Array

- MIMOSA-22THRa1 exposed to $\sim 4.4 \text{ GeV}$ electrons (DESY) in August 2013

- Analog outputs of 8 test columns (no discri.)
  - SNR with HR-18 epitaxy, at $T=30^\circ \text{C}$
    - Noise determination with beamless data taking
    - Ex: S2 ($T$ gate $L/W=0.36/1 \mu m$ against RTS noise)
      S1 ($T$ gate $L/W=0.36/2 \mu m$ against RTS noise)

- Results :
  - Charge collected in seed pixel $\sim 550 \text{ e}^-$
  - Detection efficiency of S1 & S2 $\gtrsim 99.5\%$
    while Fake rate $\lesssim O(10^{-5})$ for
    Discrimination Thresholds in range $\sim 5N \xrightarrow{>} 10N$
  - Mitigation of Fake Hits due to RTS
    noise fluctuations confirmed

  - A few $10^{-3}$ residual inefficiency may come
    from BT-chip association missmatches
    and non-optimised cluster algorithme
Spatial Resolution

• Beam test (analog) data used to simulate binary charge encoding:
  - Apply common SNR cut on all pixels using $<N>$
  - Simulate effect of final sensor discriminators
  - Evaluate single point resolution (charge sharing) and detection efficiency vs discriminator threshold for 20x20; 22x33; 20x40; 22x66 $\mu m^2$ pixels

• Comparison of 0.18 $\mu m$ technology ($>1\ k\Omega \cdot cm$) with 0.35 $\mu m$ technology ($\lesssim1\ k\Omega \cdot cm$)

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35 $\mu m$</th>
<th>0.18 $\mu m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Dim. [$\mu m^2$]</td>
<td>18.4x18.4 20.7x20.7</td>
<td>20×20 22×33 20×40 22×66</td>
</tr>
<tr>
<td>$\sigma_{sp}^{\text{bin}} [\mu m]$</td>
<td>3.2 ± 0.1 3.7 ± 0.1</td>
<td>3.2 ± 0.1 ∼ 5 5.4 ± 0.1 ∼ 7</td>
</tr>
</tbody>
</table>
CPS fabricated in 2012/13 in 0.18 μm Process

MISTRAL RO Architecture

ASTRAL RO Architecture + in-pixel amplification Optimisation

MIMOSA-22THRA
MIMOSA-22THRB
AROM-0
AROM-1
MIMOSA-32FEE
MIMOSA-32N
MIMOSA-34
MIMOSA-32 & ter

Zero Suppress Logic

SUZE02

MIMOSA-32 & -ter

LVDS

Suze 71 x 102

~1 cm

~1.3 cm² array

~1.3 cm² array

~1.3 cm² array
Depleting the sensitive layer

**DC coupling**
- Negative voltage on the anode of the collecting diode
- Transistors have negative PWELL
- $V_d \approx 2.5\text{V}$

**AC coupling**
- Anode side grounded
- Cathode side on $+HV$
- $V_d \approx 15\text{-}20\text{V}$

*Maciej Kachel*
Asynchronous Read-Out Architecture: ALPIDE

- Hierarchical readout: 1 encoder per double column (\(2^{10}\) pixels)
- 4 inputs basic block repeated to create a larger encoder
- 1 pixel read per clock cycle
- Forward path (address encoder)
- Feed-back path (pixel reset)
- Asynchronous (combinatorial) logic
- Clock only to periphery, synchronous select only to hit pixels
Asynchronous Read-Out Architecture: ALPIDE Beam Tests

- Beam tests at CERN-PS:
  - Detection performance versus discrim. threshold
    - Detection efficiency and noisy pixel rate ("fakes")
    - Sensitivity of detection efficiency to sensing node geometry and back-bias voltage (-3V)
    - Cluster multiplicity and spatial resolution (residues)

⇒ Satisfactory detection efficiency and spatial resolution observed