DAQ Systems based on NI COTS for pixels sensors characterization in beam test

CNRS  Centre National de la Recherche Scientifique (France) ~ 25 000 People
IN2P3  Institut National de Physique Nucléaire et de Physique des Particules ~ 2 500 People
IPHC  Institut Pluridisciplinaire Hubert Curien (France – Strasbourg) ~ 400 People

From the idea …

Module PXI 6585 32 I/O LVDS
Flex RIO Board PXIe 7962R

Beam Telescope @ CERN
6 Sensors Mimosa 26
8680 pictures/s → 120 MB/s

PICSEL group - ASICs Test & Characterization team
http://www.iphc.cnrs.fr/-PICSEL-.html - Gilles CLAUS – gilles.claus@iphc.cnrs.fr

DAQ : Flex RIO - PXIe
Outline

- CNRS - IN2P3 - PICSEL group - **MAPS** sensors
  - PICSEL → Physics with Integrated Cmos Sensors and ELectron machines
  - MAPS → Monolithic Active Pixels Sensor

- Digital **MAPS** readout protocol
- **COTS** for **MAPS** characterization
- **COTS** for **MAPS** applications
- Conclusion
IN2P3 – Institut National de Physique Nucléaire et de Physique des Particules
CNRS – Centre National de la Recherche Scientifique

IN2P3
20 laboratories in France – staff 2500 persons

Nuclear Physics

GANIL @ Caen
Grand Accélérateur National d’Ions Lourds

Particles Physics

LHC – CERN @ Genève
Atlas, Alice, CMS, LHCb Detectors

Astro-particles Physics

HESS Telescope
AUGER, AMS, ANTARES, GLAST

LCG : LHC Computing Grid

Calcuators Center @ Lyon
~ 200 CC all over the world

Actual developments for Future projects

➢ SLHC ➔ Super LHC
➢ ILC ➔ International Linear Collider

➢ Technical R&D ➔ Mechanic, Microelectronic, Electronic, Computing
Our challenge for future Tracking / Vertex detectors

ALICE @ LHC - 2003

1 Layer Silicon strips SSD
• 2.6.10^6 channels ~ 5 m²
• Readout ~ 153 µs

Tracking / Vertex detector?
→ Coordinates (X, Y, Z) of particles interaction point

2 Layers MAPS
• 356.10^6 channels ~ 0.16 m²
• Readout ~ 186 µs

STAR @ RHIC - 2013

Constraints in HEP → More than Moore's law!
➢ Moore → Transistors nb x 32 in 10 Years
➢ HEP → Channels nb x 100 in 10 Years ...

During ~ 10 years of R & D ...
• Area x 100 : ~ 4 mm² → 4 cm²
• Readout time / 10 : ~ 1 ms → 0.1 ms
• Radiation hardness x ~ 10
• Thinning / 10 : ~ 500 µm → 50 µm
• Analogue / Digital (Data reduction)

Staff → Total 29 – 19 Permanent staff

1990 – 2003 → Readout ASICs for LHC
➢ Design, production, test of 22 000 ASICs for ALICE

Since 1999 → R&D MAPS
➢ R&D on Monolithic Active Pixels Sensors = MAPS
➢ R&D roadmap → ILC (International Linear Collider)

More information on backup slides

IPHC - PICSEL group (Dr Winter) → One of the three Microelectronic R&D platform at IN2P3
Calibration at laboratory
Test bench $\rightarrow$ Fe$^{55}$ source
Gain [$\mu$V/e$-$] – Charge collection [%]

Detection performances measurement at CERN & DESY
Beam Telescope $\rightarrow$ $\pi$, e$^-$
Single point resolution [$\mu$m] – Detection efficiency [%]

MAPS on PCB

Fe$^{55}$ Source

MAPS

X Photons

On-line monitoring

Off-line analysis

MAPS R&D cycle $\rightarrow$ MAPS Characterization at Laboratory & in Beam test

MAPS test bench $\rightarrow$ Needs DAQ $\rightarrow$ DAQ boards developed at lab until $\sim$ 2007
Digital MAPS readout: Fast serial links 160 Mb/s ... 3.2 Gb/s

MAPS readout protocol
- Proprietary serial protocol → 4 wires
  - Clock 80-160 MHz (CLKD)
  - Synchro signal (MKD)
  - Two data lines (D00, D01)

Mimosa 26 (2009) → EUDET = R&D toward ILC (DESY – CERN)
- Area ~ 2 cm² - 663,552 Pixels
- 8680 frames / second
- Clock 80 MHz – Stream ~ 20 MB/s

The Mimosa 26 sensor (2009)
- Area ~ 2 cm² - 663,552 Pixels
- 8680 frames / second
- Clock 80 MHz – Stream ~ 20 MB/s

Proprietary readout protocol of Mimosa 26

Ultimate (2010) → STAR (BNL)
The Ultimate sensor (2011)
- Area ~ 4 cm² - 890,880 pixels
- 5388 frames / second
- Clock 160 MHz – Stream ~ 40 MB/s

Ladders of Ultimates (2011) → STAR (BNL)
2011 → Ladder of 10 x Ultimates with parallel readout
- 20 links @ 160 Mb/s = 3.2 Gb/s = 400 MB/s
Future → Concentrator ASIC → Single link
- Clock embedded in data stream → Protocol 8B10B

Sensor → 2 Links @ 160 Mb/s (40 MB/s)
Ladder → 20 Links @ 160 Mb/s (400 MB/s) = 1 Link @ 3.2 Gb/s
Mimosa 26 characterized: Lab test bench with PXI 6562 (Winter 2009)

First MAPS test bench based on COTS

- Slow Control to configure MAPS
- Mimosa 26 on PCB
- National Instruments DAQ
- PXI 6562 + CPU in PXI crate
- Data analysis software
- Discriminators “S” curves

Mimosa 26 Designed & Characterized by IPHC for EUDET (European project FP6 – R&D ILC)

- Project schedule → Run two tasks in parallel → Same deadline = Summer 2009
  - IPHC → Design & Characterization of Mimosa 26
  - INFN Ferrara → Development & Production of Mimosa 26 readout board (EUDRB VME 64x – 0 % dead time)
- No board available for Mimosa 26 characterization!

- Decision to use COTS → NI PXI 6562 board
  - Store bit stream as is on board SRAM
  - Deserialize data by software

Result → R/O development ~ 2 weeks - Mimosa 26 characterized – Drawback 94 % dead time!
Mimosa 26 validated in beam test with PXI 6562 DAQ

- But DAQ has 94% dead time → Increase data taking time
- Taking 10,000 physics events → ~140 MB data / ~2 Hours

Mimosa 26 First Application → EUDET Beam Telescope

- Beam Telescope for HEP sensors evaluation
- R&D toward ILC (http://www.eudet.org/e13/e21/)

→ COTS DAQ - 0% dead time - for EUDET Telescope copies?
**MAPS applications**: DAQ for **EUDET beam telescope**

**NI FlexRIO FPGA Modules**

- **NI PXI–795xR, NI PXIe–796xR NEW!**

  - 66 differential inputs
  - I/O adaptator module
  - LVDS → NI 6585, Analogue, etc …
  - User can develop his own module
  - User can implement his own FW
  - PXIe bus data throughput
  - PXIe x 4 ~ 800 MB/s
  - Memory → 512 MB DRAM

**Main characteristics**

- 66 differential inputs
- I/O adaptator module
- LVDS → NI 6585, Analogue, etc …
- User can develop his own module
- User can implement his own FW
- PXIe bus data throughput
- PXIe x 4 ~ 800 MB/s
- Memory → 512 MB DRAM

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**Operating Systems**
- Windows 7/Vista/XP/2000
- LabVIEW Real-Time

**Required Software**
- LabVIEW
- LabVIEW FPGA Module

**Recommended Software**
- NI FlexRIO Adapter Module Development Kit
- NI-RIO
- NI FlexRIO adapter module support

**Data throughput on PXIe bus reduce system cost!**

- A single board is needed (Not 1 board / Mimosa 26) → Reduce cost

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**Flex RIO seems to be the solution**

- FW allows on board data processing
  - On-board deserialization → Reduce SW load → 0 % dead time !
  - Handle proprietary r/o protocol → Data format, triggers etc …

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**Flex RIO FPGA Modules**

<table>
<thead>
<tr>
<th>Model</th>
<th>Bus/Form Factor</th>
<th>FPGA</th>
<th>FPGA Slices</th>
<th>FPGA DSP Slices</th>
<th>FPGA Memory (Block RAM)</th>
<th>Onboard Memory (DRAM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NI PXI–795xR</td>
<td>PXI Express</td>
<td>Virtex-5 DX6ST</td>
<td>14,720</td>
<td>640</td>
<td>8,784 kibis</td>
<td>512 MB</td>
</tr>
<tr>
<td>NI PXI–796xR</td>
<td>PXI Express</td>
<td>Virtex-5 DX6ST</td>
<td>8,160</td>
<td>288</td>
<td>4,752 kibis</td>
<td>512 MB</td>
</tr>
<tr>
<td>NI PXI–796xR</td>
<td>PXI Express</td>
<td>Virtex-5 DX110</td>
<td>12,320</td>
<td>64</td>
<td>4,038 kibis</td>
<td>128 MB</td>
</tr>
<tr>
<td>NI PXI–796xR</td>
<td>PXI</td>
<td>Virtex-5 LX85</td>
<td>12,960</td>
<td>48</td>
<td>3,856 kibis</td>
<td>128 MB</td>
</tr>
<tr>
<td>NI PXI–796xR</td>
<td>PXI</td>
<td>Virtex-5 LX90</td>
<td>7,200</td>
<td>48</td>
<td>1,328 kibis</td>
<td>128 MB</td>
</tr>
<tr>
<td>NI PXI–796xR</td>
<td>PXI</td>
<td>Virtex-5 LX301</td>
<td>4,000</td>
<td>32</td>
<td>1,152 kibis</td>
<td>0 MB</td>
</tr>
</tbody>
</table>

**01/08/2011**
National Instruments Big Physics Symposium - Austin Texas – 1, August 2011

**gilles.claus@iphc.cnrs.fr**
DAQ specifications

- Continuous readout of 6 x Mimosa 26 = 120 MB/s
- 0 % dead time → Mandatory
- Minimize manpower on FW development → Lot of students … but few engineers …

Arguments for Flex RIO / VME

- Performances → More than required (~ 800 MB/s)
- Saving manpower → No DAQ board production → Making Telescope copies consume less time
- Cost of boards is less than VME → VME boards ~ 12 K€ / Flex RIO ~ 6 K€
**EUDET Telescope DAQ: System architecture**

**DAQ → 1 Flex RIO + 1 CPU + 1 RAID**

**Two possible data output stream**

- **"Weak beam intensity"** → Data stream << 120 MB/s → Ethernet
- **"Strong beam intensity"** → Data stream ~ 120 MB/s → RAID

DAQ specifications for EUDET Telescope DAQ

- 0 % dead time → What about PXIe bus & SW latency?
- Minimize FW development time

Pragmatic approach → No time to study in details …

- Latency → Bufferize on board
  - Flex RIO has two DRAM
  - MAPS fills one DRAM / CPU reads the other
  - Filling 207 ms / Reading 84 ms
    → 123 ms margin / 207 ms = 60 % free time

- FW development time → SW development time
  - Keep FW as simple as possible → Simple HW tasks
  - Move processing to SW → Use PXIe BW & CPU Power
Firmware & Software developed at laboratory by us

- **Data deserialization**: (16 Mimosa 26 read in parallel)
- **Swap**: between the two DRAM banks (To reduce dead time risk)
- **Mimosa 26**: fill one DRAM / The second DRAM is read by SW via PXIe bus
- **Trigger handling**: Store trigger information from PMT
- **First version developed with LabVIEW FPGA**

**Serial data** (2 links at 80 MHz.)
- **deser_16_channels.vi**
- **trigger.vi**
- **Event building**
- **target_fifo_to_dram.vi**

**To internal FIFO**
- **To DRAM**
- **To PC (DMA)**

**Maximum data stream length is 1140 W16 (word of 16 bits) – 570 W16 on each link (D00, D01)**

**EUDET Telescope DAQ: General view of firmware**

Courtesy from C. Santos
EUDET Telescope DAQ: Detailed view of firmware ...

1) Deserialization one Mimosa 26

2) Deserialization 16 Mimosa 26

3) Transfer data / on board DRAM

4) Trigger handling

5) Transfer DRAM / PC DMA

FW development done by Cayetano Santos
cayetano.santos@iphe.cnrs.fr
EUDET Telescope DAQ: Status

- Flex RIO fulfilled project requirements with safety margin
  - No dead time $\rightarrow$ 60% free time – FPGA filled at $\sim$ 30%
  - System upgrade $\rightarrow$ SW upgrade (easy) / FW should not change
  - HW Evaluation + Development $\rightarrow$ $\sim$ 9 men-month (2 Engineers)

- Development & DAQ deployment
  - Development done by IPHC - Transfer to EUDET done (one week training December 2010)
  - Deployment & interface / EUDET DAQ done by EUDET collaborators
    - Integration of one Telescope DAQ is running – One more foreseen …

- Flex RIO foreseen for AIDA project
  - Readout of 72 x Mimosa 26
  - Data rate = 72 x 20 = 1440 MB/s
  - 10 X EUDET Beam Telescope data rate

AIDA $\rightarrow$ European Union project (FP7) 2011-2014
- 80 Institutes - 23 countries
  - Advanced European Infrastructures for Detectors at Accelerators
  - 9 Work Packages
    - WP9 Advanced Infrastructures for Detectors R&D
    - Task9.3 Precision Pixel Detector Infrastructures

Web $\rightarrow$ aida.web.cern.ch/aida/index.html
AIDA project DAQ (2012): **Scalability of Flex RIO architecture 😊**

**AIDA 72 Sensors → 12 Mimosa 26 / board – 2 boards / crate → 3 Crates**

- **RAID Disk - 3 TB HDD 8264**
- **HDD 8264**
- **RAID Disk - 3 TB HDD 8264**

**Specification PXIe x 4 = 4 x 200 MB/s**

**BW needed → 240 MB/s board / disk**

**PXIe Crate**
What have we **learnt** on this project?
Firmware language: **LabVIEW FPGA or VHDL?**

- **Validate** Flex RIO HW / Project specifications
  - Evaluate blocks performances \(\Rightarrow\) Deserializer, DRAM, DMA
  - LabVIEW FPGA perfect for test benches (based on NI examples)
  - LabVIEW FPGA used for the "proof of principle" DAQ FW

- **Implement more complex processing** (Trigger handling, TLU, ...)
  - Processing code written in VHDL \(\Rightarrow\) Need FW Engineer
  - "Glue code" written in LabVIEW FPGA
  - Gives a global / top view of system architecture
  - Allows non FW expert to modify system
    - Configure / disable parts, perform tests ...

- **Conclusion**
  - **LabVIEW FPGA & VHDL** are two complementary tools
  - **LabVIEW FPGA** fits well with **bottom-up approach** \(\Rightarrow\) Tests, Iterations to reach goal
Who should process data: FW or SW?

Case study → EUDET Telescope DAQ

- Deserialize data stream @ 80 MHz → FW
- Detect & store triggers information @ 2.5 MHz → FW
- Handle frame length (function of hits nb/ frame) @ 10 KHz → SW
- Handle frame format (header, data part, trailer …) @ 10 KHz → SW

First step = Keep FW as simple as possible

- PXIe bandwidth & CPU power allow to make part of processing by SW (C or LabVIEW)
- It will be easier to develop and debug SW in C / FW → Less development time 😊

Second step = Move SW processing to FW

- Split the job in small tasks → Manageable by students …
Proof of principle done 😊 … until next MAPS data throughput upgrade …

- Digital MAPS characterization → All DAQ in PICSEL group are based on NI COTS
- Digital MAPS applications → EUDET Beam Telescope

NI DAQ distribution for MAPS / Lab custom DAQ boards

- Less manpower needed → No boards production & test
- Allow to follow MAPS users request for DAQ systems …
  - Installed systems → IPNL Lyon, CEA Saclay, DESY Hambourg, … Bohn, Univ Colombia
  - Future systems → University of Bristol, Tel-Aviv, Lubiana, Copenhague … Brookhaven (BNL)

Key ideas

- Check each “fw piece” → Bottom-up approach
- Find best trade-off between FW / SW → Keep FW as simple as possible
- Focus development “Task force” To FW and SW – Reduce manpower on PCB design
Backup slides

Future HEP Projects
- SLHC → Super LHC  → Page 22
- ILC → International Linear Collider  → Page 24

Electronic for HEP at IN2P3
- Competence fields at IN2P3 for HEP detectors  → Page 25
- Microelectronic R&D at IPHC  → Page 26
- Achieved projects → ALICE & STAR vertex detectors  → Page 27

MAPS (Monolithic Active Pixels Sensors) R&D at IPHC
- PICSEL group  → Page 28
- R&D Roadmap → toward detectors for ILC  → Page 29
- Acquisition boards developed at IPHC  → Page 30

Current projects of IPHC PICSEL group
- EUDET (Physics – NI Flex RIO DAQ – INFN EUDRB DAQ)  → Page 33
- STAR Vertex Detector Upgrade  → Page 39
- AIDA  → Page 40
Future HEP Projects: The SLHC → Super LHC 1/2

SLHC-PP
Large Hadron Collider Upgrade: Preparatory Phase

Pushing the boundaries

On this site, you can read more about the changes that must be made to the LHC if the machine is to carry ten times as many protons in each beam.

Creating those stronger proton beams and then injecting them into the LHC will involve changes to the injector systems. Three new injectors will be added to the LHC: LINAC4, the Low-Power Super Proton Linac (LPSPL) and the new Proton Synchrotron (PS2).

Within the LHC itself, new and more powerful magnets will be needed to control and focus the brighter proton beams as they speed around the detector ring. You can read about the new focusing triplets, built using the latest superconducting technology.

The detectors will not escape the upgrade process. The two largest detectors at the LHC – ATLAS and CMS – will each undergo major upgrades in order to push up their sensitivity limits and make the best advantage of the higher collision rates occurring at their cores. Those changes will require new technology to power the upgraded detectors.

Finally, the new super-LHC must be robust enough to withstand a tenfold increase in radiation intensities – and the engineers working on the machine must be protected from radiation exposure.

http://slhcweb.web.cern.ch/SLHCPP
Future HEP Projects: The SLHC → Super LHC 2/2

Super Large Hadron Collider
From Wikipedia, the free encyclopedia

The Super Large Hadron Collider (SLHC) is a proposed upgrade to the Large Hadron Collider to be made after around ten years of operation. The upgrade aims at increasing the luminosity of the machine by a factor of 10, up to $10^{33}$ cm$^{-2}$s$^{-1}$, providing a better chance to see rare processes and improving statistically marginal measurements.

Many different paths exist for upgrading the collider. A collection of different designs of the high luminosity interaction regions is being maintained by the European Organization for Nuclear Research (CERN).[1] A workshop was held in 2006 to establish which are the most promising options.[2] A comprehensive press article on this workshop can be found at the CERN Courier (http://cerncourier.com/cws/article/cern/29838). A summary of the possible machine parameters can be found at Machine parameters collection (http://care-hhh.web.cern.ch/CARE-HHH/LUMI-06/lhcupgradeparameters.htm).

Increasing LHC luminosity involves reduction of beam size at the collision point and either reduction of bunch length and spacing, or significant increase in bunch length and population. The maximum integrated luminosity increase of the existing options is about a factor of 4 higher than the LHC ultimate performance, unfortunately far below the LHC upgrade project’s initial ambition of a factor of 10. However, at the latest LUMI’06 workshop,[3] several suggestions were proposed that would boost the LHC peak luminosity by a factor of 10 beyond nominal towards $10^{33}$ cm$^{-2}$s$^{-1}$.

The resultant higher event rate poses important challenges for the particle detectors located in the collision areas.[3]

Future HEP Projects: The ILC → International Linear Collider

Facts and figures
ILC by the numbers

- Cavity temperature: 2 K (-271.2 °C or -456 °F)
- Detectors: 2, based on complementary technologies
- Site: To be determined in the next phase of the project
- ILC Community: Nearly 300 laboratories and universities around the world are involved in the ILC; more than 700 people are working on the accelerator design, and another 900 people on detector development. The accelerator design work is coordinated by the Global Design Effort, and the physics and detector work by the World Wide Study.
- Collisions: Between electrons and their antiparticles, positrons, in bunches of 5 nanometres (5 billionths of a metre) in height each containing 20 billion particles and colliding 14,000 times per second
- Energy: Up to 500 billion electronvolts (GeV) with an option to upgrade to 1 trillion electronvolts (TeV)
- Acceleration Technology: 16,000 superconducting accelerating cavities made of pure niobium
- Length: Approximately 31 kilometres, plus two damping rings each with a circumference of 6.7 kilometres
- Accelerating Gradient: 31.5 megavolts per metre

→ http://www.linearcollider.org/about
Competence fields at IN2P3 for HEP detectors

- **Detectors**
  - Calorimeters
  - Vertex detectors
  - Spectrometers

- **Technical know how**
  - **Sensors** → PMT, Si strips detectors, Pixels detectors
  - **Mechanics** → Construction & system integration
  - **Electronic** → Detectors readout & Signal conditioning
    - **Discrete electronic** → Front End electronic & DAQ boards development
    - **Micro electronic** → Readout ASICs & Pixels Sensors (MAPS)
      - OMEGA group (PARIS region)
      - MICRHAU group (Rhone-Auvergne region)
      - PICSEL group (IPHC Strasbourg) – Readout ASICs – Pixels Sensors (MAPS)
Microelectronic R&D at IPHC

- Group setup in ~ 1990 → “Readout” ASICs for HEP vertex detectors (VTX)
  - Signal conditioning ASICs (C/V conversion - Analogue storage & readout)
  - Vertex detectors → micro-strip sensors → signal = charge

- ASICs Designed & Produced and Tested for HEP detectors
  - Production of ~ 4 000 ASICs (Alice128C) for STAR at RHIC - 2001
  - Production of ~ 22 000 ASICs (Hal25) for ALICE at CERN - 2003

- Since 1999 → R&D MAPS (Monolithic Active Pixels Sensors)
  - Past & future HEP detectors → Alice ~ 2,7 \(10^6\) channels / ILC ~ 300 \(10^6\) channels
  - Increase integration → Integrate detector in the ASIC – increase channels nb / ASIC
  - First HEP application → STAR VTX ~ 356 \(10^6\) pixels – 400 MAPS ~ 2012
Achieved projects ➔ ALICE & STAR vertex detectors

ALICE experiment @ LHC - CERN
- Vertex detector
- Ladder of 23 ou 26 Modules
- Module - 2 x 768 pistes
- Pitch 95 µm - Resolution ~ 20 µm
- Hybride 12 X HAL25
- External SSD layer
- 72 Ladders ~ 2,7 \(10^6\) strips ➔ 22000 r/o ASICs Hal25

STAR experiment @ RHIC - BNL
- External SSD layer
- 20 Ladders ~ 500 \(10^3\) strips ➔ 4000 r/o ASICs

ASICS ➔ R&D, Test & Production
- 2001 STAR at RHIC ~ 4000 ASICs
- 2003 ALICE at CERN ~ 22000 ASICs
- Installation / commissioning IN2P3
- IPHC – SUBATECH (Nantes)
**CMOS Sensors Group**

- IPHC (Strasbourg) → IN2P3
  - Département de Recherches Subatomiques
  - PICSEL group (Dr Marc WINTER)

- **R&D Monolithic Active Pixels Sensors → MAPS**
  - Give impact position of particles (x, y)

- R&D program started in 1999
  - More than 30 sensors designed & tested
  - From Analogue pixels matrix → Study pixels designs
  - To Digital MAPS with integrated zero suppression
    - 2009 - Mimosa 26 → EUDET (FP6) Beam Telescope
    - 2010 - Ultimate → STAR Vertex Detector upgrade

- Group organization
  - Microelectronic design → 10 Engineers
  - Sensors characterization → 5 Engineers
  - Students → ~ 7 PhD

**The sensor: Pixels matrix**

- Analogue MAPS → Serial analogue readout
- Digital MAPS → One comparator / column
- Smart MAPS → Integrated zero suppression logic

**During 10 years of R & D …**

- Area x 100 : ~ 4 mm² → 4 cm²
- Readout time / 10 : ~ 1 ms → 0.1 ms
- Radiation hardness x ~ 10
- Thinning / 10 : ~ 500 µm → 50 µm

**Sensors Applications**

- **Futur Vertex Detectors: STAR – ILC – CBM**

  - ILC Vertex Detector: 5 Layers of MAPS ~ 300 10⁶ pixels
  - Example: ILC
    - ~ 300 10⁶ pixels
    - Pitch 20-10 µm
    - Readout time 25-200 µs
    - 50 KRad/an
    - $10^{11}$ n_{eq}/cm²/an
The main goal: the ILC ➔ Achieve the goal by successive performance steps

- Apply MAPS technology to other experiments ➔ Constraints delayed in time

EUDET 2007/2009
Beam Telescope

- Projet FP6 EUDET (DESY-Hamburg, Germany)
  - Area: 6 x 2 cm²
  - Readout speed: Ana. 20 MHz ➔ Num @ 80 MHz
  - Temperature & power: No constraint

- STAR Experiment (RHIC – Brookhaven, USA)
  - Area: ~1600 cm²
  - Readout speed: Ana. 20 MHz ➔ Num @ 160 MHz
  - Temperature & power: 30°C - 100mW/cm²

- CBM Experiment (GSI – Darmstadt, Germany)
  - Area: ~500 cm²
  - Readout speed: N, 15 x 10⁹ pixels/sensor/s
  - Rad Tol: 1 MRad, > 10¹³ Nₑq/cm²

- Experiments at ILC
  - 5-6 detection layers: ~3000 cm²
  - Readout speed: N, 15 x 10⁹ pixels/sensor/s
  - Temperature & power: 30°C - 100mW/cm²
  - Rad Tol: ~300 kRad, ~10¹² Nₑq/cm²
PICSEL Group → Acquisition boards development at IPHC – VME ADC 2000

Analog
- Up to 16 ADC 12 bit 20 Mhz

Digital
- External Trigger handling
- Pattern Generator

Daq : PC & VME
- 4 Mo / s VME bus - Ethernet 6 Mo / s

- MAPS Ctrl signals
- 4 Inputs
- Up to 256 k pixels / Input
- Readout 1-20 Mhz
- Dynamic 2000 mV
- Resolution 512 µV
- Noise 400 µV
- Linearity ~ 0.3 %
Why a New DAQ?

- Very Low Data Bandwidth 4 MB/s
- MAPS Digital outputs – No way
- Readout frequency Max 20 Mhz
- On Board Data Sparcification – No way
- More generic sequencer (MAPS Digital Ctrl)
- Software … Linux … Windows …

Status?

- Board Ready
- Lab MAPS test bench operationnal (Summer 2005)
- Final IReS USB DAQ Software for Summer 2006
  - Multiple boards … USB bandwidth …
  - Dynamic Variable Size event data format
  - Windows ROOT monitoring
- Generic sequencer for end of Summer 2006

DAQ USB 2.0

- Analog
  - 1-4 ADC 12 bits – 50 Mhz
  - 1 ADC 14 bits – 100 MHz
  - $10^6$ pixels shared 1-4 Inputs
- Digital
  - Pattern generator & Trigger
  - 16 Digital inputs
- Daq
  - Transfer 15 MB/s USB 2.0
- Firmware (To Be Done)
  - CDS Calculation (Done)
  - Pedestal substraction
  - Data sparification
Digital front end for USB ADC

**DAQ requirements**
- 16 LVDS inputs @ 40 MHz

**What is available**
- USB ADC board 4 channels - 12 bits @ 50 MHz

**Solution?**
- Bypass one ADC → 16 LVTTL digital inputs
- Develop an interface board → LVDS / LVTLL
- Add clock distribution → Multi boards synchronization
EUDET → European Union project (FP6) 2006-2010
31 Institutes - 12 countries
Detectors R&D towards the International Linear Collider

NA1 → Management of I3
NA2 → Detector R&D Network
TA1 → Access to DESY test Beam Facility
TA2 → Access to R&D Infrastructure
JRA1 → Test Beam Infrastructure
JRA2 → Infrastructure for Tracking Detectors
JRA3 → Infrastructure for Calorimeters

→ www.eudet.org
EUDET beam telescope

Reference planes of EUDET Beam Telescope
- Supported by EU FP6.
- Infrastructure to support the ILC detector R&D.
- Specifications:
  - Extrapolated resolution <2 μm.
  - Sensor area ~2 cm².
  - Read-out speed ~ 10 kframes/s.
  - Up to 10⁶ hits/s/cm².

Commissioning @ CERN-SPS last year:
- BT completely equipped with MIMOSA-26.
- Largely used by ILC and non-ILC groups.

www.eudet.org

Presentation done at EUDET meeting 13/04/2010
by Rita De Masi

Full talk → http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=86593
Two possible data output stream

- **Weak beam intensity** → Data stream << 120 MB/s → Ethernet
- **Strong beam intensity** → Data stream ~ 120 MB/s → RAID
EUDET Telescope DAQ: FW → Data streams & Clock rates ...

Uo to 16 x Mimosa 26

Deserializers

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Deser 16 bits

Access → W128 @ 20 MHz

(16 Mi26 x 80 Mb/s x 2 links / 128 bits)

MAPS fills DRAM 1

➢ 1800 frames → 207 ms

➢ 6 x Mimosa 26 = 24 MB

CPU reads DRAM 2

➢ Read 24 MB @ 200 MB/s

➢ Read done in 84 ms

➢ 207 – 84 = 123 ms margin

➢ 123 ms ⇔ 60 % CPU Free

DRAM 1 – 256 MB 128 bits

Word 0 (Low 64)

Word 0 (High 64)

Word 1 (Low 64)

Word 1 (High 64)

Memory 128 bits

Access → W128 @ 12.5 MHz

CPU PXIe 8130

CPU reads DRAM 2

➢ Read 24 MB @ 200 MB/s

➢ Read done in 84 ms

➢ 207 – 84 = 123 ms margin

➢ 123 ms ⇔ 60 % CPU Free

DRAM 2 – 256 MB 128 bits

Word 0 (Low 64)

Word 1 (High 64)

Word 2 (Low 64)

Word 3 (High 64)

Memory 128 bits

Access

~ 200 MB/s

Access → W128 @ 12.5 MHz

Access → Bit @ 80 MHz

Access → W16 @ 5 MHz
EUDET Telescope Demonstrator – VME DAQ

EUDRB board - A VME64x-based DAQ card for MAPS sensors – INFN Ferrra

Mother board built around an ALTERA CycloneII FPGA (clock rate: 80MHz) and hosting the core resources and interfaces (VME64X slave, USB2.0, EUDET trigger bus).

NIOS II, 32 bit “soft” microcontroller (clock rate: 40Mz)

implemented in the FPGA for

• on board diagnostics
• on-line calculation of pixel pedestal and noise
• remote configuration of the FPGA via RS-232, VME, USB2.0

Two readout modes:

Zero Suppressed readout to minimize the readout dead-time while in normal data taking.

Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations.

Analog daughter card based on the successful LEPSI and SUCIMA designs clock rate up to 20 MHz

digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link

Courtesy from A.Cotta Ramusino & C.Bozzi - http://www.fe.infn.it/u/bozzi/Talk_HH.ppt
EUDET Memos on Beam Telescope performances

- Web page → http://www.eudet.org/e26/e28/
  - Eudet-Memo-2009-25 → Final sensor performances validation

EUDET Memos on EUDRB board

- Web page → http://www.eudet.org/e26/e28/e182
  - /e615/Eudet_Memo-2008-38 → Status 2008

EUDET Memos on IPHC NI Flex RIO DAQ for Beam Telescope

- Web page → http://www.eudet.org/e26/e28/
  - Eudet-Memo-2010-25 → System overview
  - Eudet-Memo-2010-26 → Source tree installation
  - Eudet-Memo-2010-27 → DAQ emulator
  - Eudet-Memo-2010-28 → LabVIEW demonstration software
Current project ⇒ STAR vertex detector upgrade

STAR experiment ⇒ BNL (Brookhaven National Laboratory)
- Upgrade of vertex detector (traces)
- Add two layers of pixels sensors (MAPS) ⇒ 2012 – 2013
  - Two concentric layers covered with sensors
  - 400 sensors ULTIMATE de 2 cm x 2 cm area

Two concentric layers covered with sensors
- Length 20 cm
- Radius 2.5 cm & 8 cm
- Area 1600 cm² covered with 400 sensors 2 cm x 2 cm
- Data flow max ~ 16 GB/s

http://www.iphc.cnrs.fr/Presentations.html
Advancing European detector development

The AIDA project addresses infrastructures required for detector development for future particle physics experiments. In line with the European strategy for particle physics, AIDA targets user communities preparing experiments at a number of key potential future accelerators: SLHC (luminosity-upgraded LHC), future Linear Colliders (ILC and CLIC), future accelerator-driven neutrino facilities or future B-physics facilities (e.g. Super-B).

The infrastructures covered by the AIDA project are key facilities required for an efficient development of the future experiments, such as: test beam infrastructures (at CERN and DESY), specialised equipment irradiation facilities (in several European countries), common software tools, common microelectronics tools and engineering coordination offices. The project, coordinated by CERN, involves more than 80 institutes and laboratories from 23 countries as beneficiaries or associate partners. Read more >>

DESY wire chamber, courtesy of Interactions
AIDA task 9.3

Precision pixel detector infrastructure

• subtask 9.3.1: telescope infrastructures
  • pixel telescope (TimePix, ATLAS FE-14, MIMOSA)
  • CO₂ cooling plant
  • common DAQ (DESY, Geneva)
• subtask 9.3.2: system integration
  • infrastructure for the evaluation of thermo-mechanical performances

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Telescope for alignment issues

- Bristol, DESY, Geneva, Oxford, Strasbourg, Warsaw, ...
- Large Area Telescope (LAT)
- Thin removable target
- Alignment Investigation Device (AID)

- Large area Telescope (6 planes)
  - Extension of EUDET Beam Telescope
  - One plane surface $\sim 25$ cm$^2$
    - 4 x Ultimate
    - 15 x Mimosa

- Flex RIO foreseen for AID box
  - 6 double side ladders
  - Each ladder = 6 Sensors Mimosa 26
  - Total $\Rightarrow$ 6 ladders x 2 sides x 6 sensors = 72 sensors

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EUDET meeting, Geneva 13/04/2010

Courtesy from R. De Masi
Large Area Telescope

Baseline: extension of EUDET-BT

- 2x2 (or 3x3) ULTIMATE sensor
- 20.8 μm pixel pitch with binary output
- ~2x2 cm² active area each
- readout time < 200 μs
- 50 μm thin

Or …

- MIMOSA-26 like
- pitch 16 μm → ~3.5 μm spatial resolution
- 3000 x 3000 pixels (~ 5x5 cm²)
- proof of principle of stitching
- readout time <= 300 μs (2-sides read-out)
- windowing for collimated beam → ~50-80 μs r.o. time
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Alignment Investigation Device

- Alignment and vertexing capabilities
- Double-sided vs. single sided
- Powering of the system
- Air flow cooling effects
- ...

EUDET meeting, Geneva 13/04/2010

Courtesy from
R. De Masi