DATA ACQUISITION SYSTEM BASED ON NI COTS FOR PIXELS SENSORS CHARACTERIZATION IN BEAM TEST

G.Claus, C.Santos, IPHC Strasbourg France - On behalf of PICSEL & Microelectronic groups.

Abstract

This paper will present the migration from custom DAQ boards developed in HEP (High Energy Physics community) for MAPS [1] (Monolithic Active Pixels Sensors) readout to COTS (Components Off The Shelves) solutions based on the NI FlexRIO PXIe architecture. The MAPS sensors generate digital data stream at up to 160 MHz frequency rate and data throughput from 120 MB/s to few GB/s. The presentation will focus on the DAQ system for the EUDET [2] beam telescope [3] project, which is the first application of MAPS sensors in HEP field.

RESARCH CONTEXT

A long term R&D program on MAPS is running at IPHC (Institut Pluridisciplinaire Hubert Curien) since 1999. The final goal is to fabricate sensors which fit with the vertex detectors requirements of the future HEP particle accelerators: ILC [4] (International Linear Collider) and SLHC [5] (Super LHC). The vertex detector measures X, Y, Z coordinates of particles generated by beams collision. As MAPS are 2D sensors, giving X, Y coordinates, concentric layers of MAPS are used to get Z coordinate.

This R&D program requires microelectronic design and sensors characterization activities, both are done within the PICSEL group (Physics with Integrated Cmos Sensors and ELectron colliders) at IPHC. Since 2009 all sensors technology and architecture validation steps have been passed, and first sensors Mimosa 26 [6] and Ultimate with signal digitization and data flow reduction on chip have been designed. They are foreseen for the EUDET beam telescope and the STAR vertex detector upgrade [7] which are intermediate validation steps of our R&D program toward ILC and SLHC vertex detectors. These sensors require reliable DAQ systems able to acquire fast digital serial links. A PXIe DAQ architecture based on NI FlexRIO board (PXIe 7962R) has been setup, evaluated and validated for MAPS sensors steering and readout.

EUDET BEAM TELESCOPE

The EUDET project is an European Union project (FP6 2006-2010) which aims to provide characterization infrastructures to sustain detectors R&D toward the ILC. The beam telescope is one of the equipments delivered to HEP community by the EUDET collaboration.

The telescope characterizes two main parameters of the detector: the spatial resolution and the detection efficiency. The spatial resolution is the error on the particle position detection. Its value is function of detector pitch, usually 2-4 µm. The detection efficiency is the ratio between particles number detected by the sensor to the real number of particles passing through it. This important parameter is required to be better than 99,5 %.

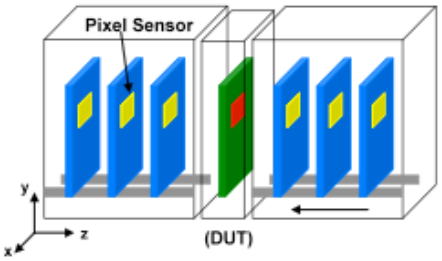

Figure 1 : Schematic view of EUDET Beam Telescope

The figure 1 shows the beam telescope composed by six reference pixels sensors and the DUT (Device Under Test) to characterize. The particle beam used to characterize the DUT is 120 GeV pions at CERN SPS or 1-6 GeV electrons at DESYII. The coordinates of particle track passing through the telescope are calculated from the X, Y coordinates given by the six reference sensors. The spatial resolution and detection efficiency are processed by comparison of the information given by the DUT to the one given by the telescope. The statistic required for the calculation is a few thousands of tracks.

BEAM TELESCOPE DEMONSTRATOR

A first telescope version, the demonstrator [8], has been setup in 2008 with MimoTel, a reference sensor with analogue outputs. It has been used by five different groups (CALICE HCAL, DEPFET, MimoRoma, LCFI, SiLC) of HEP community. The DAQ was based on the EUDRB [9] VME-64x board developed by our collaborators from INFN Ferrara (figure 2).

Figure 2 : EUDRB VME board – INFN Ferrara

This board acquires analogue links of MimoTel at 20 MHz over 12 bit resolution. It applies an efficient on line pixels selection algorithm in order to reduce the data stream.

FINAL BEAM TELESCOPE

The reference sensor, Mimosa 26, for the final telescope has been designed in 2009 by PICSEL group. It has been integrated in the EUDET beam telescope in 2010. Mimosa 26 includes signal digitization and the pixels selection algorithm previously done by the EUDRB board. This new sensor improves the telescope frame rate from 1 kHz to 10 kHz.

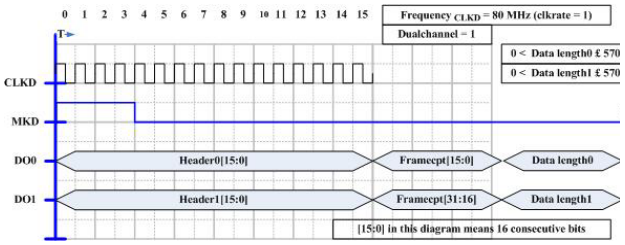

Figure 3 : Mimosa 26 readout protocol

Mimosa 26 provides a digital serial link on four wires: a clock (CLKD) at 80 MHz, a synchronization signal (MKD) and two data links (D00, D01). The sensor generates a frame each 115,2 µs, but the useful data part of the frame depends on the particle rate. Therefore the data stream varies between 0 and 20 MB/s per sensor, which translates to 120 MB/s for the telescope equipped with six sensors. One has to mention, that the EUDRB board has been upgraded via a digital daughter board in order to acquire Mimosa 26 serial links.

The final beam telescope provides a spatial resolution of ~ 2 µm and can reach close to 10 000 frames/s [10]. It has been widely used by HEP community since summer 2010. Therefore, it has become necessary to duplicate this telescope, but as EUDET project ended in December 2010, there was no human resources to produce and test new EUDRB boards. As PICSEL group already had knowledge in COTS DAQ, it has been charged to study a DAQ solution for the telescope copies.


Figure 4 : EUDET beam telescope

NI FLEX RIO DAQ PROPOSAL

A DAQ solution based on the NI PXIe FlexRIO board PXIe 7962R and the LVDS front-end module PXI 6585 has been proposed, setup and validated.


Figure 5 : FlexRIO PXIe 7962R and LVDS module

The DAQ specifications were to acquire six Mimosa 26, which corresponds to 12 LVDS links at 80 MHz, handle serial proprietary protocol and sustain a data throughput of 120 MB/s without any dead time. The proposed architecture should easily overcome all these requirements as the LVDS front-end has 16 links at up to 200 MHz, the PXIe 7962R has a data throughput of 800 MB/s on the PXIe bus and an on board firmware can be implemented to handle the proprietary serial protocol.

NI FLEX RIO VALIDATION TEST

In order to check if the FlexRIO on board hardware fulfilled the project requirement, a test bench has been setup. The goal was to measure the maximum writing frequency to the on board DRAM from the LVDS front-end and the data throughput on the PXIe bus. This test has been done in the worst conditions, without data deserialization by the firmware, in order to have the highest memory access frequency.

The data from Mimosa 26 has been acquired at 80 MHz into the on board DRAM. Each 1800 frames, corresponding to 207 ms of acquisition time, the readout was stopped, the data were transferred to the CPU, deserialized and compared to expected pattern. This test has been performed on 20×10^6 frames without any error, which corresponds to ten times the usual statistic needed for the sensor characterization. A data throughput of 195 MB/s has been measured on the PXIe bus. This result is in good agreement with PXIe x1 specifications (200 MB/s) which is more than needed for the application. We also have done a test with 4 DMA channels running in parallel and reach close to 800 MB/s which corresponds to the PXIe x4 specifications.

These results confirm that the PXIe FlexRIO board is a viable solution for the EUDET telescope DAQ.

SYSTEM DESIGN DECISIONS

In order to get quickly an operational system and to minimize the firmware development time it has been decided to split the data processing tasks between firmware and software. The data deserialization at 80 MHz and the trigger signal detection at up to 2,5 MHz are performed by firmware. The proprietary data format with

variable frame length is handled by the software running on the PXIe CPU board. Another reason for this choice is the flexibility given to the DAQ users to upgrade the data formatting code in order to get the best interface with their DUT DAQ without the need of firmware development knowledge. The firmware has been coded in LabVIEW FPGA. The data processing has been written in C code within a DLL and LabVIEW has been used for top level software and GUI.

On hardware point of view it has been decided to bufferize data on board instead of using direct streaming through the PXIe bus. The cycle is done in 207 ms, corresponding to the acquisition of 1800 frames, the CPU reads DRAM in 84 ms which lets 123 ms of free time margin. This architecture reduces the consequences of bus or software latency. It also avoids arbitration problems on DRAM between write and read cycle, which makes it possible to increase the access frequency.

SYSTEM ARCHITECTURE

One single PXIe crate (Figure 6) hosts the DAQ system composed of the PXI 6585 LVDS front-end, the FlexRIO acquisition board PXIe 7962R, the PXIe 8130 CPU and an interface board PXI 8262 to the RAID system. The data are either sent to the EUDET top level run control and monitoring software via a gigabit Ethernet link or to a RAID system if needed.

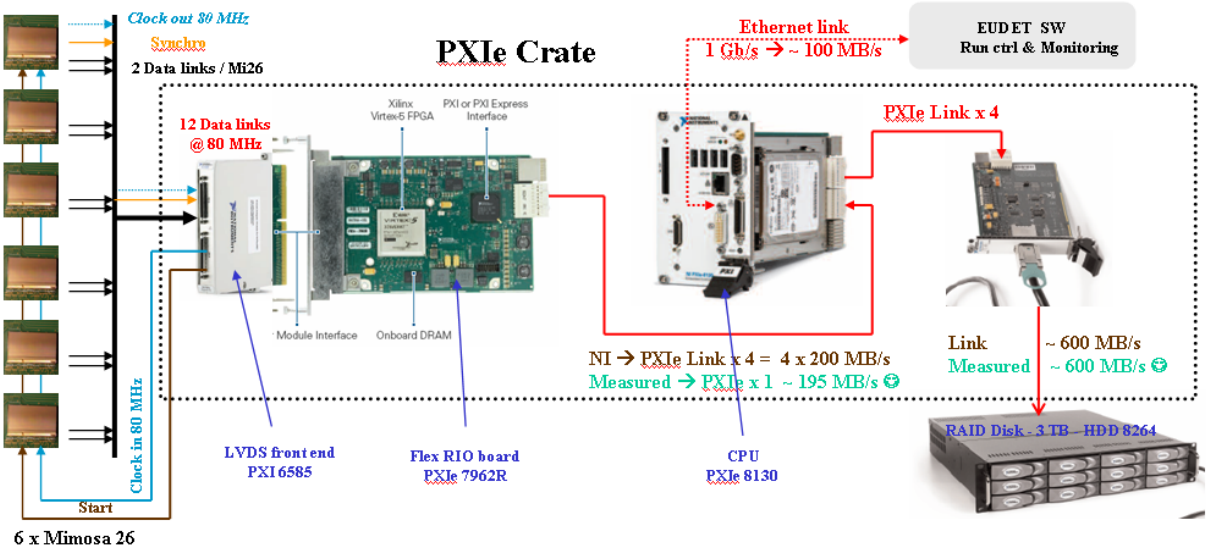

Figure 6 : EUDET Telescope DAQ based on PXIe Flex RIO architecture

FIRMWARE ARCHITECTURE

Two data processing tasks are implemented by firmware: Mimosa 26 readout and the trigger handling. A schematic view of firmware is shown on figure 7.

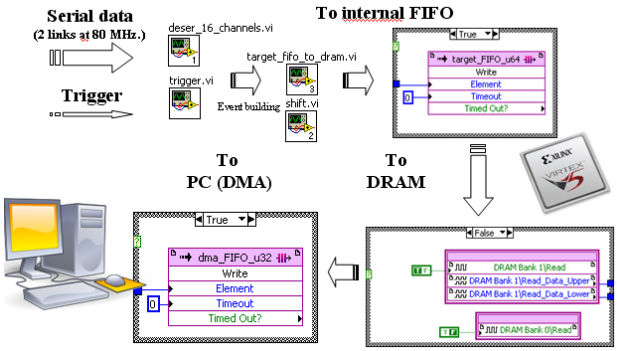

Figure 7 : Firmware architecture

The first task of the firmware is Mimosa 26 readout. It deserializes data at 80 MHz, stores them in one DRAM bank, while it sends the content of second DRAM bank to the CPU via DMA access through the PXIe bus. As the Mimosa 26 data format is organized in sixteen bits words on two links, it has been decided to keep this architecture and use one sixteen bits deserializer per link. Therefore it will be easy to implement further on-line processing at frame level. As, up to sixteen Mimosa 26 can be acquired by the board, therefore thirty two deserializers are needed.

The second task of the firmware is the trigger handling. It detects a trigger signal occurrence and makes time stamping with 12,5 ns resolution. The firmware also reads the TLU [11] (Trigger Logic Unit) which is a trigger board developed by the EUDET collaboration.

The proof of principle firmware version has been developed in LabVIEW FPGA to get quickly a running system. Now, complex processing parts have been

written in VHDL via the user defined CLIP (Component-Level IP) interface.

SOFTWARE ARCHITECTURE

The GUI and a board control API have been developed with LabVIEW. The data processing tasks like frame format and variable frame length handling are done by functions calls from a DLL written in C. The data stream is therefore either sent on gigabit Ethernet link or stored on RAID system. A multithreading architecture has been used in order to run in parallel data processing and storage on disk.

This software implementation allows either to store raw data stream (120 MB/s) as is or to extract only the useful part of information. This processing reduces the data rate by one order of magnitude (~12 MB/s).

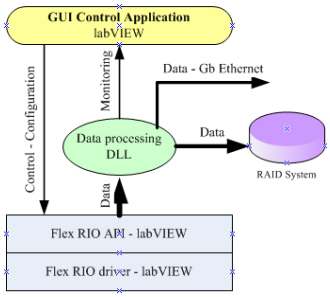

Figure 8 : Software architecture

SYSTEM PERFORMANCES

The DAQ is able to acquire six Mimosa 26 at full data stream (120 MB/s) and save the data on disk without any dead time. It still has 22 ms free time on a

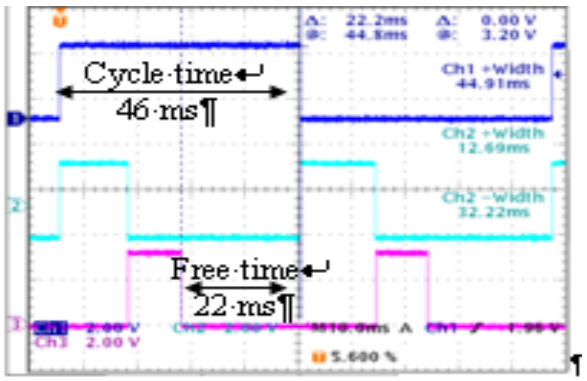

Figure 9 : CPU free time at full load (120 MB/s)

46 ms (400 frames) cycle time (figure 10) which means 48 % of free CPU time. On figure 10, the trace N° 1 shows the acquisition cycle (46ms), this is the time between two edges. The trace N° 2 represents the board readout time (14 ms) to CPU DRAM while trace N° 3 shows the data processing time by the software (10 ms). On firmware point of view, the Flex RIO FPGA is filled only at 30 % which lets margin for further data processing implementation.

An upgrade of this DAQ has been done for a telescope equipped with Ultimate sensors. They provide data on two serial links at 160 MHz and generate a total data stream of 230 MB/s which has been acquired without any dead time.

CONCLUSION

The presented NI COTS architecture based on the PXIe FlexRIO 7962R board and the PXIe 8130 CPU fulfils EUDET beam telescope DAQ requirements with safety margins on FPGA and CPU usage. Moreover, COTS products like the Flex RIO board and the LVDS front-end are cheaper than home made acquisition boards production and test.

Firmware and software development time, including learning NI LabVIEW FPGA and FlexRIO validation tests is estimated to nine men-months.

The project has been successfully transferred to our EUDET collaborators via a DAQ training week [12] organized in December 2010. The integration in the EUDET telescope DAQ software is currently running.

The modularity of the PXIe FlexRIO platform and its high data throughput makes it scalable for future DAQ systems. It is foreseen for the AIDA [13] (FP7) project which is the continuation of EUDET but with DAQ constraints one order of magnitude higher: 1,4 GB/s.

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