Mimosa 34 description

**Tower CIS March 2013 submission:**

- 32 blocks of 64 rows x 16 columns
  - 30 Source Follower blocks for charge collection tests
  - **Purpose** ➔ charge sensing dependence on pixel dimensions & diode parameters
- 2 Pre-Ampli inverter blocks

**Integr. Time:**
- Source Follower: 32 µs (at 2 MHz input clock)
- Pre-Ampli: 10 µs (at 6.25 MHz input clock)
Mimosa 34 description

Sensor steering signals
(Same pinout that mimosa32Ter)

Power
The analog GND are not display here

Analog Ref
Specific Vdiode depletion for P13

Array Address: static
Output Buffer current

Digital Inputs
Line Reset*
Clamping (Ampli)
Input Clock

Digital

Analog Data Outputs
(*16)

Analog
1.8 Volts

Outputs markers

Pads output
For diode pad protection

Analog
3.3 Volts*

*signal or alimentation connected but not needed for this sensor
Mimosa 34 description

Marker in/out
Steering signal
Static address

Output 0-15

polarization

polarization
**Mimosa 34 description**

**Basic block:** 16 columns x 64 rows
16 parallel analog outputs

**Reference Analog Voltage Settings**

<table>
<thead>
<tr>
<th>Definition</th>
<th>Typical value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iref</td>
<td>~50 µA</td>
</tr>
<tr>
<td>Vclp (pre_ampli)</td>
<td>~1 V</td>
</tr>
</tbody>
</table>

**Analog_out bus (x16)**

**Total:** 32 arrays (2 INV and 30 SF)
### Mimosa 34 description

#### SF Arrays structure

<table>
<thead>
<tr>
<th>Pixel</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>P4</th>
<th>P5</th>
<th>P6</th>
<th>P7</th>
<th>P8</th>
<th>P9</th>
<th>P10</th>
<th>P11</th>
<th>P12</th>
<th>P13</th>
<th>P14</th>
<th>P15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch (x)</td>
<td>33</td>
<td>44</td>
<td>66</td>
<td>33</td>
<td>44</td>
<td>66</td>
<td>33</td>
<td>44</td>
<td>66</td>
<td>33</td>
<td>44</td>
<td>66</td>
<td>33</td>
<td>30</td>
<td>27</td>
</tr>
<tr>
<td>N(D)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>F(D)</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>11</td>
<td>11</td>
<td>15</td>
<td>11</td>
<td>11</td>
<td>15</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>S(D)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>11</td>
<td>11</td>
<td>8</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>11</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

- **Pixel staggered**
  - ✓
  - ✓
  - ✓
  - ✓
  - ✓

- **Others**
  - DPW/8col
  - DPW/8col
  - LRT
  - DPW/8col
  - upw
  - N\(_{\text{diff}}\)
  - N\(_{\text{diff}}\)
  - AC
  - FBD

### Pitch (y) = 33

<table>
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<tr>
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<td>11</td>
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<tr>
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<td>15</td>
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<td>8</td>
<td>8</td>
<td>2</td>
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- **Pixel staggered**
  - ✓
  - ✓
  - ✓

- **Others**
  - LRT
  - N\(_{\text{diff}}\)
  - N\(_{\text{diff}}\)
  - FBD

### Pitch (y) = 22

- **N(D)** = Number of sensing diodes in the pixel (1 or 2)
- **F(D)** = Footprint of diode, viz. section of volume in which the sensing diode is integrated : 15 or 11 μm²
- **S(D)** = Surface of diode : 15, 11, 8, 5, 2 & 1 μm²
- **LRT** = Large Reset Transistor : wide gate (2 time longer) against RTS noise
- **N\(_{\text{diff}}\)** = Diode different that standard the Nwell, less deep
- **FBD** = Forward Bias Diode replacing reset transistor, (Self_Bias)
- **DPW/8col** = the first 8 columns are with full DeepPWell except an opening of 8*8 μm bellow the diode
Mimosa 34 description

15 SF structures 33µm height:
- P1_33µm_3T_N(1)_F(15)_S(8u)_DPW/8col
- P2_44µm_3T_N(1)_F(15)_S(8u)_STG
- P3_66µm_3T_N(1)_F(15)_S(8u)_STG
- P4_33µm_3T_N(1)_F(11)_S(11u)_DPW/8col
- P5_44µm_3T_N(1)_F(11)_S(11u)_STG
- P6_66µm_3T_N(1)_F(15)_S(8u)_STG_LRT
- P7_33µm_3T_N(1)_F(11)_S(5u)_DPW/8col
- P8_44µm_3T_N(1)_F(11)_S(5u)_STG
- P9_66µm_3T_N(2)_F(15)_S(5u)_
- P10_33µm_3T_N(1)_F(11)_S(2u)_DPW/8col
- P11_44µm_3T_N(1)_F(11)_S(2u)_STG_Ndiff
- P12_66µm_3T_N(2)_F(11)_S(2u)_Ndiff
- P13_33µm_SB_N(1)_F(11)_S(11u)_AC
- P14_30µm_3T_N(1)_F(11)_S(8u)_STG
- P15_27µm_SB_N(1)_F(11)_S(8u)_STG

15 SF structures 22µm height:
- P17_33µm_3T_N(1)_F(11)_S(11u)_STG
- P18_44µm_3T_N(1)_F(11)_S(11u)_STG
- P19_66µm_3T_N(1)_F(15)_S(15u)_STG
- P20_33µm_3T_N(1)_F(11)_S(8u)_STG
- P21_44µm_3T_N(1)_F(11)_S(8u)_STG
- P22_66µm_3T_N(1)_F(15)_S(8u)_STG_LRT
- P23_33µm_3T_N(1)_F(11)_S(2u)_STG
- P24_44µm_3T_N(1)_F(11)_S(5u)_STG
- P25_66µm_3T_N(2)_F(15)_S(5u)_
- P26_33µm_3T_N(1)_F(11)_S(2u)_STG_Ndiff
- P27_44µm_3T_N(1)_F(11)_S(1u)_STG_Ndiff
- P28_66µm_3T_N(2)_F(15)_S(2u)_
- P29_33µm_SB_N(1)_F(11)_S(11u)_STG
- P30_30µm_3T_N(1)_F(11)_S(8u)_STG
- P31_27µm_3T_N(1)_F(11)_S(8u)_STG

2 Pre-Ampli structures
- P0_33*20µm_2Diodes_11u
- P16_22*20µm_1Diode_11u

- N(D) = Number of sensing diodes in the pixel (1 or 2)
- F(D) = Footprint of diode, viz. section of volume in which the sensing diode is integrated : 15 or 11 µm²
- S(D) = Surface of diode : 15, 11, 8, 5, 2 & 1 µm²
- LRT = Large Reset Transistor : wide gate (2 times longer) against RTS noise
- N_{diff} = Diode different that standard the Nwell, less deep
- FBD = Forward Bias Diode replacing reset transistor, (Self_Bias)
- DPW/8col = the first 8 columns are with full DeepPWell except an opening of 8*8 µm bellow the diode
- STG = The diode inside the pixel is staggered

Pre-amplifier with an optimize inverter from Mi32Ter with two types of amplifier
8 columns of each type
Mimosa 34 description

Footprint of Diode
Surface of Diode

P23 (diode footprint=11µm² surface=2µm²)
Diode staggered pixel to pixel

P17 (22*33 µm)  
P20 (22*66 µm)
Mimosa 34 description

Diode surface variation

P17 (diode footprint=11µm², surface=11µm²)
P23 (diode footprint=11µm², surface=2µm²)
P20 (diode footprint=11µm², surface=8µm²)
P26 (diode footprint=11µm², surface=2µm², Nwell less deep)
**Mimosa 34 description**

**P13_33μm_SB_N(1)_F(11)_S(11u)_AC**

For this matrix with AC coupling $V_{diodeHV}$ can be set until 5 Volts.
To avoid to perturb the other neighboring pixels around, we set a one pixel ring with no diode around this matrix.

⇒ On the 16col*64row matrix only 14col*62row are active pixels.
Pixels read-out description
Mimosa 34 description

Source Follower pixels
- 3T and SelfBias readout

For all the 3T sub-Matrices the reset transistor is connect in permanent reloading (similar behavior of a diode)
Mimosa 34 description

SF pixel array steering (clock frequency : 2 MHz)

Individual Pixel Array:
16 columns x 64 rows (lines)

64 bit Shift Register:
one “hot bit”

*signal connected but not needed for this sensor

Analog_out bus (x16)
Mimosa 34 description

SF pixel array steering (clock frequency : 2 MHz)
Self-bias mode: 3T reset transistors in diode setting (permanently “on”)

Integration time (64 clock pulses)

Clock
Sync
Out
In

Out may be shorted to In on the PCB

The CDS is done by subtracting two consecutive frames
Mimosa 34 description
Mimosa 34 description

Pré-Ampli area: clamping pixels (P0, P16)
Mimosa 34 description

Ampli pixel array (clock frequency: 6.25 MHz)

Individual Pixel Array: 16 columns x 64 rows (lines)

64 bit Shift Register: two “hot bits”
64 bit Shift Register: one “hot bit”

Analog_out bus (x16)
Ampli Pixel array steering
(clock frequency : $100/16 = 6.25$ MHz)

Integration time (64 clock pulses)

First row
Clock

Sync

Clp

Pixel sampling

Out (Pout)

Out (Pout) may be shorted to In (Pin) on the PCB

In (Pin)
Mimosa 34 description

First sampling Read the pixel value
Reload the capacitance with Vclamp
Second sampling Base line reference (Calib)

Pixel line 63

Pixel line 0

Marker from the sensor
Sampling clock
Data from one output
Clamping signal
Clock send to the sensor

Read Clp Calib
PCB description and Schematic
Mimosa 34 description
**Mimosa 34 description**

For matrix P13 (page10)
The diode is polarize at 5V
When not use this bias can be fix to 0V

**MI34DAC**

Dac on Aux board
Vdiode SF $\rightarrow$ Vclp_discri
Vclp $\rightarrow$ Vclp
Iref $\rightarrow$ Iref

Vref_buf $\rightarrow$ Vref

Vdiode_Amp $\rightarrow$ Vref2 connected but not used

Vbsf $\rightarrow$ Vref1