Mimosa32Ter: Tower CIS, July 2\textsuperscript{nd} 2012 submission: 6 Metal, MiM Capacitor, Quadruple Well (deep-N and deep-P wells)
- Overall chip dimension: \(3.3 \times 13.5 = 44.5\, \text{mm}^2\)
- HiRes (18\,\mu m) and Standard (8\,\mu m) epitaxial layer

\begin{itemize}
  \item \textbf{CERN Test Structures}
  \item \textbf{Diodes&Ampli: charge collection and radiation hardness study}
  \item \textbf{Discri in_pixels}
\end{itemize}

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Diodes & Amplifier area

32 Basic block: 16 columns x 64 rows
Basic pitch: 20x20 µm
16 parallel analog outputs,
5 bit (static) address to connect single block to the output bus.
Integr. time 32 µs (&2 MHz)
15 SF structures 20x20µm:
- P1_SFter_2T_elt_11u
- P2_SFter_3T_lin_11u (M32_P6)
- P3_SFter_3T_linSmall_11u_DPW33u
- P4_SFter_3T_elt_11u_DPW33u
- P5_SFter_3T_linSmall_11u
- P6_SFter_3T_linSmall_11u
- P7_SFter_3T_linSmall_11u_FullDPW_06
- P8_SFter_3T_linSmall_11u_FullDPW_010
  - P9_SFter_2T_lin_11u
  - P10_SFter_2T_linSmall_11u
  - P11_SFter_2T_linSmall_11u
  - P12_SFter_2T_ACmim_linSmall_11u
  - P13_SFter_2T_ACmim_linSmall_11u
- P14_SFter_2T_linSmall_11u_NoPwellAround
  - P15_SFter_2T_linSmall_15u

15 Ampli structures: (9 from Andrei, 5 from IRFU & 1 from Maciej)
- P16_mk_InvAmp
- P17_ad_nmos_fd
- P18_ad_nmos_fd_psw
- P19_ad_ncmos3p3_fd
- P20_ad_nmos_ft
- P21_ad_nmos_bt
- P22_ad_nmos3p3_fd
- P23_yd_SF_CDS
- P24_ad_nmos3p3_ft
- P25_ad_ncmos_fd
- P26_ad_ncmos_ft
  - P27_PMOS_5
- P28_yd_PMOS_5_Fbmod
- P29_FG_nmos_AC
- P30_yd_pmos_5_noFB

2 SF pitch 20x33 µm:
- P31_SingleDiode_interleaved
  - P31_DoubleDiode

All transistors STD!
No Low leakage (hvt)
Mimosa32Ter, Submitted July 2nd 2012

Diodes & Amplifiers Area

Clock @ 2MHz

Read-out @ 6.25 MHz

Physics with Integrated CMOS Sensors and Electron Machines
Mimosa32Ter: proposed changes

- Separation Vdiode/Vclamp: done
- Resistor protected pads for analog IO: done except on 16xAnOut
  - Additional AVDD: +3.3 V: done
CERN Block

- Would like to better understand influence of:
  - Pixel pitch
  - Spacing of collection electrode to surroundings
  - Collection electrode shape and size
  - Bias
  - Integration time
  - …
- Already some indication that optimization of these parameters may have large influence on power-performance, essential for architecture choice.
**Principle of matrix readout**

- Double correlated sampling with signal storage on storage capacitors just after reset and at the end of the integration time
- Readout afterwards

A test matrix allowing full decoupling between integration time and readout time
Cross section

**nwell diode**

\[ p^+ : -30 \text{ V}; \; n^+ : 0 \text{ V} \]

- \( p \)-epi
  - depleted volume

**nwell with deep pwell in the between**

- \( p \)-epi
  - depleted volume

Measurements: **Breakdown** voltage and depletion layer capacitance

- NW width: 1 \( \mu \text{m} \) or 2 \( \mu \text{m} \)
- NW with DPW width: up to 3.40 \( \mu \text{m} \)
Each block has an individual power supply and it can be tested individually.