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Annexe to the User Manual of Mimosa22

Mimosa22ter

(Preliminary version)

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Document history		
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1.0	June 2009	Annexe to the User Manual of Mimosa22

Mimosa22ter chip			
Version	Date	Description	Comments
1.0	Submitted May 09	AMS 035 Opto Version, 576 x 136 pixels	Preliminary version

Mimosa22ter

Note:
The paragraphs which are modified from the user manual of Mimosa22 are shown in grey.
The modifications or additions are written in red.

1 Introduction

Mimosa22ter is a Mimosa22-like prototype including a new pixel array and the possibility to generate on-chip the voltage for pixel clamping.
Mimosa22ter has been designed in AMSC35B4O1 CMOS-Opto 0.35 µm. This CMOS-Opto_process has 4 metal layers and 2 poly layers, and uses 14 µm epitaxial wafers. The Process Design Kit V3.70 has been provided by CMP. The design tools are CADENCE DFII 5.1 with ASSURA and CALIBRE rules. The chip has been submitted in a Multi Chip Run via CMP the 29 may 2009 in the run A35C09_3.

Mimosa22ter has the following characteristics:

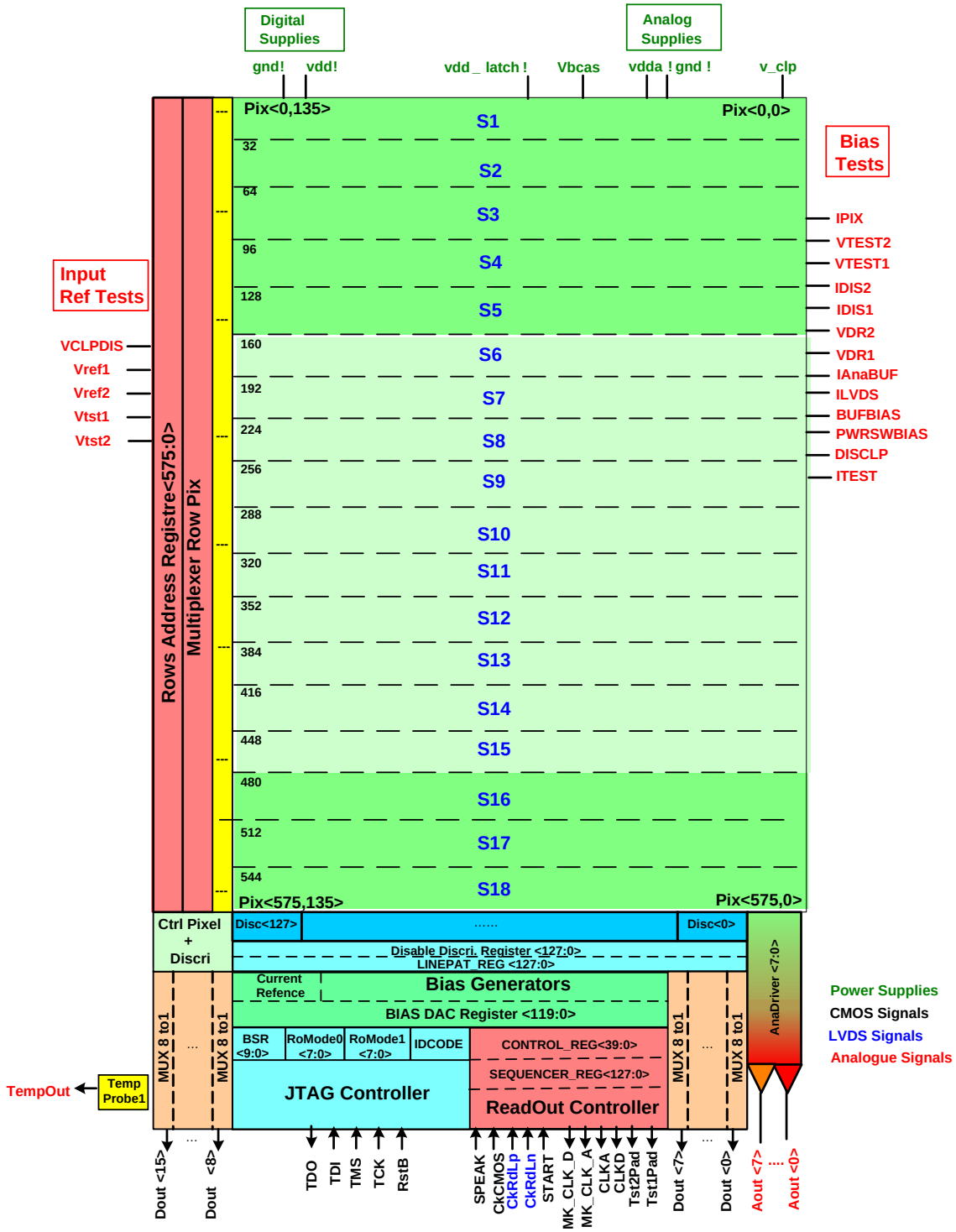
- The sensor matrix is divided in 18 groups of 32 rows each. Each row is composed of 136 pixels of 18.4 µm pitch. The table presented on page 5 summarizes the main characteristics of pixel groups.

- Mimosa22ter includes a linear regulator to generate on-chip the voltage for pixel clamping.
  This voltage can be adjustable by a 4 bit DAC. In a flexible way, this block can be disable by JTAG and the clamping voltage can be then provided via the PAD named «v_clp».

- The Pad Ring is compatible with the existing version of test board. The modification are:
  The VKIMMO, RADTOLPIXGATE and TempOutUp Pads have been suppressed.
  The vdd_diode Pad has been renamed in Vbcas Pad.
  The Vbcas voltage is the voltage needed for the cascode transistor in pixel.

- Two test circuits, a PLL and a DLL have been included nearby the Mimosa22ter core. These circuits have each one their independent Pad Ring.

This documentation presents only the modifications and additions implemented in Mimosa22ter. See the user manual of Mimosa22 named «Mimosa22_v1_Doc.doc» to have more information how to operate Mimosa22ter.



Mimosa22ter functional view
Does not correspond to the floorplan neither for the core, neither for the pad ring

Submatrixes of Pixels in Mimosa22ter					Comments
Sub-matrix	Row address range	Name	ENC, e	Conv., uV/e	
S1	0-31	CAS_FT_FELT_C3	12.4	193.6	like S3, but the feedback filter capacitance is 3 times larger
S2	32-63	CAS_FELT_FELT_C3	12.2	184.0	like S5, but the feedback filter capacitance is 3 times larger
S3	64-95	CAS_FT_FELT_C1	12.1	192.7	like S6, but the forward diode replaced by FELT
S4	96-127	CAS_FELT_FELT_C1_RTGS	12.1	179.1	like S5, but the distance to diffusion around diode is reduced
S5	128-159	CAS_FELT_FELT_C1	12.1	179.1	like S9, but the forward diode replaced with ELT
S6	160-191	CAS_FT_FD_C1	6.5	174.9	like S9, but FELT replaced by standard transistor
S7	192-223	CAS_FT_FD_C3	6.6	176.6	like S6 but the feedback filter capacitance is 3 times larger
S8	224-255	CAS_FELT_FD_C3	7.4	140.9	like S9, but the feedback filter capacitance is 3 times larger
S9	256-287	CAS_FELT_FD_C1	7.7	127.4	**like S15, but the cascode amplifier used instead of common source, the basic structure for all cascode designs**
S10	288-319	CAS_FELT_FD_C1_RTGS	7.7	127.4	like S9, but the distance to diffusion around diode is reduced
S11	320-351	CAS_FELT_FD_C3_CLL	7.9	132.2	like S9, but the feedback filter capacitance is 3 times larger and clamping capacitance is larger
S12	352-383	CAS_FELT_FD_C1_CLL	8.3	121.0	like S9, but the clamping capacitance is larger
S13	384-415	M22bisS2	10.7	132.1	copy of Mimosa22bis S2
S14	416-447	CS_FT_FD_C1	11.2	91.6	like S15, but standard transistor instead of ELT
S15	448-479	CS_FELT_FD_C1	11.2	83.6	**similar to S13 but diode is 3.65x3.65um, diodes is the basic structure for the other groups (except S13)**
S16	480-511	CAS_FELT_FELT_C1_CLL	13.5	163.7	like S5, but clamping capacitance is larger
S17	512-543	CS_FT_FELT_C1	19.4	83.5	like S14, but the forward diode replaced with ELT
S18	544-575	CS_FELT_FELT_C1	19.5	80.7	like S15, but the forward diode replaced with ELT

Summary of pixel matrix

2 Control Interface

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2.2.5 BIAS_DAC Register

The BIAS_DAC register is 120 bit wide; it sets simultaneously the 15 DAC registers.
As show bellow these 8-bit DACs set voltage and current bias. After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit. The current values of the DACs are read while the new values are downloaded during the access to the register. An image of the value of each DAC can be measured on its corresponding test pad.

Bit range	DAC #	DAC Internal Name	DAC purpose	Corresponding Test Pad
119-105	DAC14	VclpPix	On-chip generation of pixel clamping voltage	v_clp
111-104	DAC13	IPIX	Pixel source follower bias	IPIX
103-96	DAC12	IVTST2	Test Level, emulates a pixel output	VTEST2
95-88	DAC11	IVTST1	IDEM	VTEST1
87-73	DAC10	IDIS2	Discriminator bias 2	IDIS2
79-72	DAC9	IDIS1	Discriminator bias 1	IDIS1
71-64	DAC8	IVDREF2	Discriminator Reference 2	VDREF2
63-56	DAC7	IVDREF1	Discriminator Reference 1	VDREF1
55-48	DAC6	IAnaBUF	Analogue Buffer bias	IAnaBUF
47-40	DAC5	ILVDS	LVDS PAD bias	ILVDS
39-32	DAC4	ID2PWRS	Discriminator bias 2 (mode low consp.)	
31-24	DAC3	ID1PWRS	Discriminator bias 1 (mode low consp.)	
23-16	DAC2	IBufBias	Ref&Tst Buffer bias	BUFBIAS
15-8	DAC1	IPwrSWBias	Discriminator Power Pulse bias	PWRSWBIAS
7-0	DAC0	ICLPDISC	Discriminator Clamping bias	DISCLP

2.2.7 RO_MODE1 Register

The RO_MODE1 registers are 8 bits large; they allow selecting specific analogue mode of the chip.

Bit #	Bit Name	Purpose	Basic configuration value	
7	NU4	Reserved, Not Used		
6	NU3	Reserved, Not Used		
5	NU2	Reserved, Not Used		
4	DisBufRef	Disable the internal reference	0	Select Internal Buffer
3	DisVcpPix	Disable the on-chip generation of the pixel clamping voltage	0	Normal mode : the on-chip voltage generation is active
2	En_AOP_Disc	Enable the Power pulse Amplifier	0	Normal mode
1	En_Pulse_Discri	Enable the discri power pulse mode	0	Normal mode
0	En_TstDis	Enable the discri. test mode	0	Normal mode

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3.2 Biasing Mimosa22ter

The BIAS_DAC register has to be loaded before operating Mimosa22.
The 15 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	Simulation			Resolution	Range	Experimental
	$Code_{16}$ - $Code_{10}$	DacInternal current-µA	Output value			$Code_{16}$ - $Code_{10}$
VclpPix (1)	04-04		2.1 V	20 mV	From 2 up to 2.3 V	
IPIX	32-50	50	50 µA	1 µA	From 0 up to 255 µA	
IVTST2	71-113	113	1.182 V	10 mV	From 1 up to 1.5 V	
IVTST1	8C-140	140	1.183 V	250 µV	From -30 up to 34 mV	
IDIS2	20-32	32	5 µA	156 nA	From 0 up to 255 µA	
IDIS1	20-32	32	10 µA	312 nA	From 0 up to 255 µA	
IVDREF2	71-113	113	1.182 V	10 mV	From 1 up to 1.5 V	
IVDREF1(2)	80-128	128	1.182 V	250 µV	From -30 up to 34 mV	
IAnaBUF	32-50	50	500 µA	10 µA	From 0 up to 255 µA	
ILVDS	20-32	32	7 µA	218 nA	From 0 up to 255 µA	
ID2PWRS	A-10	10	100 nA	10 nA	From 0 up to 255 µA	
ID1PWRS	A-10	10	100 nA	10 nA	From 0 up to 255 µA	
IBufBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA	
IPwrSWBias	A-10	10	10 µA	1 µA	From 0 up to 255 µA	
ICLPDISC	64-100	100	2.1 V	10 mV	From 1.2 up to 3.2 V	

(1) The DAC «IKIMMO» has been replaced by the 4 bit DAC VclpPix. The 4 MSB bits are not used and has to be set to 0.

(2) Referenced with respect to IVDREF2. The threshold voltage of the discriminators ΔVth is defined as Vref1-Vref2 (Vref1=Vref2+ΔVth).

4 Pad Ring

The pad ring of Mimosa22ter is build with

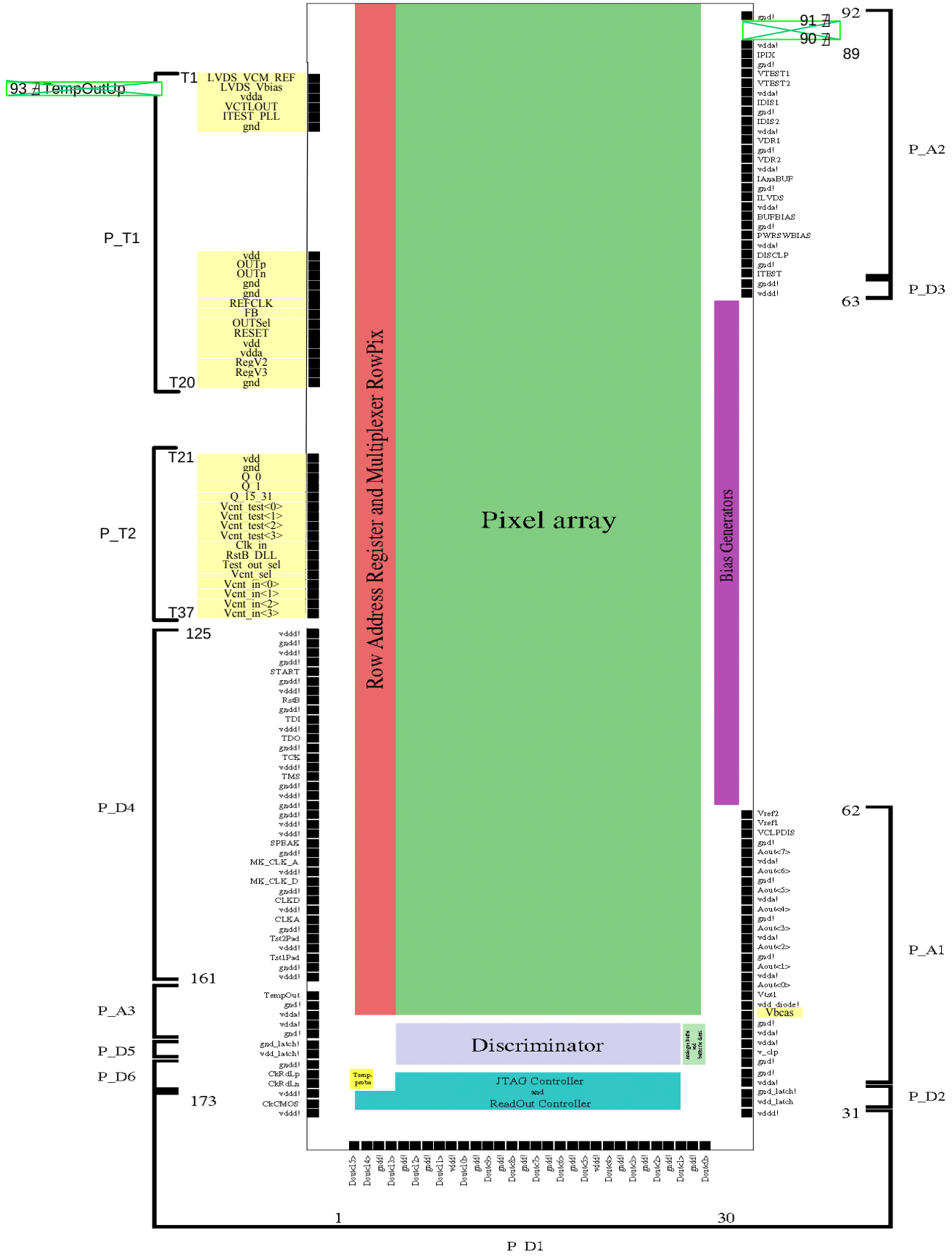
- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 7 functional independent parts

- CMOS JTAG and Test purpose pads
- LVDS Read Out Drivers
- Digital outputs
- Read Out Analogue Outputs
- Bias Test
- Analogue and Digital Power supplies
- Test Circuits

Each part has its own supply pads.

4.1 Mimosa22ter Pad Ring and Floor Plan View



4.2 Pad List

The bonding of the power supply pads specified in green colour is mandatory

Pad ring segment 1 – P_D1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
1	Dout<15>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 127-120
2	Dout<14>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 119-112
3	gnd	Output buffer ground	GND3OP	Output buffer ground
4	Dout<13>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 111-104
5	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
6	Dout<12>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 103-96
7	gnd	Output buffer ground	GND3OP	Output buffer ground
8	Dout<11>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 95-88
9	vdd	Output buffer supply	VDD3OP	Output buffer supply
10	Dout<10>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 87-80
11	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
12	Dout<9>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 79-72
13	gnd	Output buffer ground	GND3OP	Output buffer ground
14	Dout<8>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 71-64
15	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
16	Dout<7>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 63-56
17	gnd	Output buffer ground	GND3OP	Output buffer ground
18	Dout<6>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 55-48
19	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
20	Dout<5>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 47-40
21	vdd	Output buffer supply	VDD3OP	Output buffer supply
22	Dout<4>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 39-32
23	gnd	Output buffer ground	GND3OP	Output buffer ground
24	Dout<3>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 31-24
25	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
26	Dout<2>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 23-16-
27	gnd	Output buffer ground	GND3OP	Output buffer ground
28	Dout<1>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 15-8
29	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
30	Dout<0>	Tri-State Output Buffer, 2 mA	BT2P	Digital Output ch. 7-0
31	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
173	CkCMOS	Clock buffer, 2 mA	ICCK2P	CMOS clock
174	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core

Pad ring segment 1 – P_D2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
32	vdd_latch	Core logic and periphery cells supply	AVDD3ALLP	Supplies periphery & core only for LATCH
33	gnd	Core logic and periphery cells ground	AGND3ALLP	Ground periphery & core only for LATCH

Pad ring segment 1 – P_A1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
34	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
35	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
36	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
37	v_clp		APRIOP	Clamping voltage for pixel array
38	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
39	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
40	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
41	Vtst2		APRIOP	External injection of Vtest2
42	Vbcas		APRIOP	Cascode voltage for pixel
43	Vtst1		APRIOP	External injection of Vtest1
44	Aout<0>		APRIOP	Analogue output
45	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
46	Aout<1>		APRIOP	Analogue output
47	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
48	Aout<2>		APRIOP	Analogue output
49	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
50	Aout<3>		APRIOP	Analogue output
51	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
52	Aout<4>		APRIOP	Analogue output
53	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
54	Aout<5>		APRIOP	Analogue output
55	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
56	Aout<6>		APRIOP	Analogue output
57	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
58	Aout<7>		APRIOP	Analogue output
59	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
60	VCLPDIS		APRIOP	External injection of Discri clamping
61	Vref1		APRIOP	External injection of Discri Ref1
62	Vref2		APRIOP	External injection of Discri Ref2

Pad ring segment 1 – P_D3				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
63	vdd	Core logic and periphery cells ground	AVDD3ALLP	Ground periphery & core only for DAC
64	gnd	Core logic and periphery cells supply	AGND3ALLP	Supplies periphery & core only for DAC

Pad ring segment 1 – Test_PLL_T1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
65	ITEST	Analog I/O pad, 0 Ω serial	APRIOP	Reference current (1µA)
66	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
67	DISCLP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Output for Discri Clamping
68	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
69	PWRSWBIAS	Analog I/O pad, 0 Ω serial	APRIOP	Discri Power Pulse Voltage Bias
70	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
71	BUFBIAS	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Ref&Tst Buffer voltage bias
72	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
73	ILVDS	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: LVDS PAD voltage bias
74	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
75	IAnaBUF	Analog I/O pad, 0 Ω serial	APRIOP	Analogue Output Buffer bias
76	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
77	VDR2	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Reference 2
78	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
79	VDR1	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Reference 1
80	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
81	IDIS2	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Bias 2
82	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
83	IDIS1	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Discriminator Bias 1
84	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
85	VTEST2	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: VTEST2
86	VTEST1	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: VTEST1
87	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
88	IPIX	Analog I/O pad, 0 Ω serial	APRIOP	DAC output: Pixel Array Bias
89	vdda	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
~~90~~	~~VKIMMO~~	~~Analog I/O pad, 0 Ω serial~~	~~APRIOP~~	~~A reference voltage from DAC output~~
~~91~~	~~RADTOLPIXGATE~~	~~Analog I/O pad, 0 Ω serial~~	~~APRIOP~~	~~POLY Gate voltage for Andrei RadTol Pix~~
92	gnd	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core

Note: The pads «VKIMMO» and «RADTOLPIXGATE» have been suppressed.

Pad ring segment 1 – P_D4				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
125	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
126	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
127	vdd	Output buffer supply	VDD3OP	Output buffer supply
128	gnd	Output buffer ground	GND3OP	Output buffer ground
129	START	CMOS Input Buffer	ICP	Readout: Input synchronisation
130	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
131	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
132	RstB	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Asynchronous Active Low Reset
133	gnd	Output buffer ground	GND3OP	Output buffer ground
134	TDI	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
135	vdd	Output buffer supply	VDD3OP	Output buffer supply
136	TDO	Tri-State Output Buffer, 4 mA	BT4P	JTAG Serial Data Out
137	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
138	TCK	CMOS Clock Input Buffer, 2 mA	ICCK2P	JTAG Clock
139	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
140	TMS	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
141	gnd	Output buffer ground	GND3OP	Output buffer ground
142	vdd	Output buffer supply	VDD3OP	Output buffer supply
143	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
144	gnd	Output buffer ground	GND3OP	Output buffer ground
145	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
146	vdd	Output buffer supply	VDD3OP	Output buffer supply
147	SPEAK	CMOS Input Buffer	ICP	Active Readout Marker & Clock
148	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
149	MK_CLK_A	Tri-State Output Buffer, 2 mA	BT2P	Readout: Analogue Marker & Clock
150	Vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
151	MK_CLK_D	Tri-State Output Buffer, 2 mA	BT2P	Readout: Digital Marker & Clock
152	gnd	Output buffer ground	GND3OP	Output buffer ground
153	CLKD	Tri-State Output Buffer, 2 mA	BT2P	Readout Digital clock
154	vdd	Output buffer supply	VDD3OP	Output buffer supply
155	CLKA	Tri-State Output Buffer, 2 mA	BT2P	Readout Analogue clock
156	gnd	Core logic and periphery cells gnd	GND3RP	Digital ground, periphery & core
157	Tst2Pad	Tri-State Output Buffer, 2 mA	BT2P	Readout Test Pad
158	vdd	Core logic and periphery cells supply	VDD3RP	Digital supply, periphery & core
159	Tst1Pad	Tri-State Output Buffer, 2 mA	BT2P	Readout Test Pad
160	gnd	Output buffer ground	GND3OP	Output buffer ground
161	vdd	Output buffer supply	VDD3OP	Output buffer supply

Pad ring segment 1 – P_A3				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
162	TempOut	Direct Pad, no protections	DIRECTPAD	Temperature probe output
163	gnd	Core logic and periphery cells ground	AGND3ALLP	Ground periphery & core
164	vdda	Core logic and periphery cells supply	AVDD3ALLP	Supplies periphery & core
165	vdda	Core logic and periphery cells supply	AVDD3ALLP	Supplies periphery & core
166	gnd	Core logic and periphery cells ground	AGND3ALLP	Ground periphery & core

Pad ring segment 1 – P_D5				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
167	vdd	Core logic and periphery cells supply	VDD3ALLP	Supplies periphery & core for DAC
168	gnd	Core logic and periphery cells gnd	GND3ALLP	Ground periphery & core for DAC

Pad ring segment 1 – P_D6				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
169	gnd	Core logic and periphery cells ground	GND3ALLP	Ground periphery & core
170	CkRdLp	LVDS In +	Full Custom	Readout Clock Signal
171	CkRdLn	LVDS In -	Full Custom	Readout Clock Signal
172	vdd	Core logic and periphery cells supply	VDD3ALLP	Supplies periphery & core

Pad ring segment 1 – P_T1 (PLL)					
Pad	**Name**	**PCB Name**	**Pad General Function**	**PadType**	**Function for the chip**
T1	LVDS_VCM _REF	LVDS_VCM _REF	Analog I/O pad, 0 Ω serial	APRIOP	Common mode voltage for LVDS driver
T2	LVDS_Vbias	LVDS_VBIAS	Analog I/O pad, 0 Ω serial	APRIOP	Bias current for LVDS driver
T3	vdda	AVDD_2	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core
T4	VCTLOUT	VCTLOUT	Analog I/O pad, 0 Ω serial	APRIOP	Buffered control voltage
T5	ITEST_PLL	ITEST_PLL	Analog I/O pad, 0 Ω serial	APRIOP	Output of the internal current reference
T6	gnd	AGND_2	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core
T7	vdd	VDD_LVDS	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core only for LVDS
T8	OUTp	PLL_OUTp	LVDS Out+	Full Custom	PLL output Clock
T9	OUTn	PLL_OUTn	LVDS Out-	Full Custom	PLL output Clock
T10	gnd	GND_LVDS	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core only for LVDS
T11	gnd	DGND_2	Core logic and periphery cells gnd	GND3ALLP	Digital Ground output buffers, periphery &core
T12	REFCLK	REFCLK	CMOS Clock input buffer, 2 mA	ICCK2P	PLL input Clock
T13	FB	FB	Output buffer, 2 mA	BU4P	Feedback clock
T14	OUTSel	OUTSEL	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Output select: When OUTSel is 0, output is reference clock, and internal buffer of control voltage is powered down. When OUTSel is set to 1, output is VCO clock. This port could be used to test LVDS driver.
T15	RESET	RSTB_PLL	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Reset: low active. When reset is low, divider is reset and loop filter is discharged.
T16	vdd	DVDD_2	Core logic and periphery cells supply	VDD3ALLP	Digital Supplies output buffers periphery & core
T17	vdda	AVDD_REG	Core logic and periphery cells supply	AVDD3ALLP	Analogue Supplies periphery & core only for regulator
T18	RegV2	REGV2	Analog I/O pad, 0 Ω serial	APRIOP	Regulator output, 2.5V
T19	RegV3	REGV3	Analog I/O pad, 0 Ω serial	APRIOP	Regulator output, 3V
T20	gnd	AGND_REG	Core logic and periphery cells gnd	AGND3ALLP	Analogue Ground periphery & core only for regulator

Pad ring segment 1 – P_T2 (DLL)					
Pad	**Name**	**PCB Name**	**Pad General Function**	**PadType**	**Function for the chip**
T21	vdd	DVDD_3	Core logic and periphery cells supply	VDD3ALLP	Digital Supplies output buffers, periphery & core
T22	gnd	DGNG_3	Core logic and periphery cells gnd	GND3ALLP	Digital Ground output buffers, periphery &core
T23	Q_0	Q_0	Output buffer, 2 mA	BU2P	The first output of the digital controlled delay line (DCDL) in digital DLL
T24	Q_1	Q_1	Output buffer, 2 mA	BU2P	The second output of the DCDL in digital DLL
T25	Q_15_31	Q_15_31	Output buffer, 2 mA	BU2P	The last output of the DCDL in digital DLL
T26	Vcnt_test<0>	VCNT_TEST<0>	Output buffer, 2 mA	BU2P	Test outputs of digital controlled numbers: when Test_out_sel is "High", Vcnt_test<3:0> are connected to the outputs of the up/down counter; when Test_out_sel is "Low", Vcnt_test<3:0> are connected to the outputs of digital filter (the average numbers of the maximum values and minimum vanues of the counter when DLL is locked.)
T27	Vcnt_test<1>	VCNT_TEST<1>	Output buffer, 2 mA	BU2P	
T28	Vcnt_test<2>	VCNT_TEST<2>	Output buffer, 2 mA	BU2P	
T29	Vcnt_test<3>	VCNT_TEST<3>	Output buffer, 2 mA	BU2P	
T30	Clk_in	CLK_IN	CMOS Clock input buffer, 4 mA	ICCK4P	Input reference clock
T31	RstB_DLL	RSTB_DLL	CMOS Input Buffer, Pull Up	ICUP	Reset signal of DLL
T32	Test_out_sel	TEST_OUT_SEL	CMOS Input Buffer, Pull Up	ICUP	Select signal of the Vcnt_test
T33	Vcnt_sel	VCNT_SEL	CMOS Input Buffer, Pull Up	ICUP	Select signal of the Vcnt_in
T34	Vcnt_in<0>	VCNT_IN<0>	CMOS Input Buffer, Pull Down	ICDP	Input digital controlled signals of DCDL: When Vcnt_sel is "High", Vcnt_in<3:0> are connected to the outputs of the up/down counter; When Vcnt_sel is "Low", Vcnt_in<3:0> are connected to the external input signals
T35	Vcnt_in<1>	VCNT_IN<1>	CMOS Input Buffer, Pull Down	ICDP	
T36	Vcnt_in<2>	VCNT_IN<2>	CMOS Input Buffer, Pull Down	ICDP	
T37	Vcnt_in<3>	VCNT_IN<3>	CMOS Input Buffer, Pull Down	ICDP	