Development of CMOS Pixel sensors (CPS) for vertex detectors in present and future collider experiments

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On behalf of IPHC-Strasbourg group (CNRS & Université de Strasbourg)

• CMOS pixels sensors
  ➢ Main features and state of the art
  ➢ STAR PXL detector
  ➢ ILD VTX detector

• Toward new applications
  ➢ 0.18 μm technology
  ➢ ALICE ITS upgrade
  ➢ Lab & beam test results

• Summary
CMOS pixel sensor (CPS) for charged particle detection

- **Main features**
  - Monolithic, p-type Si
    - Signal created in low doped thin epitaxial layer \(\sim 10-20 \mu m\)
    - \(\sim 80 \text{e-} /\mu m\) \(\Rightarrow\) total signal \(\sim O(1000 \text{e-})\)
  - Thermal diffusion of e-
    - Limited depleted region
    - Interface highly P-doped region: reflection on boundaries
  - Charge collection: N-Well diodes
    - Charge sharing \(\Rightarrow\) resolution
  - Continuous charge collection
    - No dead time

- **Main Advantages**
  - Granularity
    - Pixel pitch down to \(10 \times 10 \mu m^2\) \(\Rightarrow\) spatial resolution down to \(\sim 1 \mu m\)
  - Material budget
    - Sensing part \(\sim 10-20 \mu m\) \(\Rightarrow\) whole sensor routinely thinned down to 50 \(\mu m\)
  - Signal processing integrated in the sensor
    - Compacity, flexibility, data flux
  - Flexible running conditions
    - From \(\leq 0^\circ C\) up to 30-40\(^\circ C\) if necessary
    - Low power dissipation \((\sim 150-250 \text{mW/cm}^2)\) \(\Rightarrow\) material budget
    - Radiation tolerance: \(\gg 100s \text{kRad and } O(10^{12} \text{neq}) \Rightarrow f(T,pitch)\)
  - Industrial mass production
    - Advantages on costs, yields, fast evolution of the technology, Possible frequent submissions

- **Main limitation**
  - Industry addresses applications far from HEP experiments concerns
    - Different optimisations on the parameters on the technologies
  - Recently: new accessible processes:
    - Smaller feature size, adapted epitaxial layer
    - Open the door for new applications
State of the art (1)

- IPHC-Strasbourg and collab.
  - CPS developed since ~ 1999
  - Typical performances in AMS 0.35 μm technology
    - Detection efficiency $\geq 99.9\%$ with fake rate $\leq 10^{-5}$
    - Typical spatial resolution (20 μm pitch):
      - $\sim 1.5 \mu m$ (analog output)
      - $\sim 3.5 \mu m$ (digital output)

- Read-out architecture with digital output
  - In pixel preamplification and CDS
  - Column parallel rolling shutter read-out
    - Continuous read-out
    - Integration time = #rows x row r.o. time (100ns)
    - End-of-columns discriminators
    - Data sparsification (0-suppression)
    $\Rightarrow$ enhances r.o. speed with preserving material budget, granularity and power consumption
State of the art (2): current applications

• EUDET pixel telescope
  - Beam telescope (FP6 project)
  - 6 x Mimosa-26 planes (// r.o. and dig output)
  - Successfully operating since 2008

• STAR PXL detector
  - First vertex detector equipped with CPS
    - 2 layers = 40 ladders x 10 sensors
    - First sectors (3/10) installed May 2013
    - Commissioning completed
    - End of construction under way

• Prototype: Mimosa-28 (Ultimate)
  - AMS 0.35 μm techno with high resistivity epitaxial layer
  - 960 x 928 pixels, 20.7 μm pitch ⇒ 3.8 cm²
  - In pixel CDS & ampli, column parallel read-out
  - End of column discrim. and binary charge encoding
  - On chip zero suppression
Mimosa-28 (=Ultimate) performances

- Operating conditions
  - JTAG + 160 MHz
  - Temperature
    - 35°C
  - Read-out time = 200 μs
    - Suited to ≥ 10⁶ part/cm²/s
  - Power consumption
    - 150 mW/cm²

- Performances
  - Noise ~ 15 e⁻ ENC @ 35°C
  - Eff vs fake rate
  - Spatial resolution
    - charge sharing
    - σ_sp ≥ ~ 3.5 μm
  - Radiation tolerance
    - 3.10¹² n_eq/cm² + 150 kRad @ 35°C

⇒ reached performances meets specifications
CPS and vertex detector optimisation: squaring the circle

- **Vertex detector design and specifications**
  - Physics performances
    - Spatial resolution
    - Material budget ↔ multiple scattering
  - Experimental environment constraints
    - Radiation hardness (ionising and non ion. rad.)
    - Occupancy ↔ Read-out speed
    - Power dissipation ↔ cooling?
  - Other parameters
    - Costs, fabrication reliability and flexibility
    - Mechanical integration
    - Geometry
    - Alignment issues

- **Interdependence of these parameters**
  - e.g. lower radius of inner layer
    - Better $\sigma_{\text{i.p.}}$ but larger occupancy, higher rad.
    - Needs higher read-out speed and/or granularity ⇒ power dissipation

⇒ CPS presents an attractive trade off with respect to all these parameters
An example of vertex detector optimisation: ILD @ ILC

- **Baseline:** (cf. ILC - Detector Baseline Document)
  - Spatial resolution/material budget \( \sigma_b < 5 + 10/\rho \beta \sin^{3/2} \theta \mu m. \)
  - Occupancy 1st layer: ~ 5 part/cm^2/BX \( \Rightarrow \) few % occupancy max
  - Radiations: O(100 krad) et O(1x10^{11} n_{eq} (1MeV)) / year
  - Power dissipation: 600W/12W (Power cycling, ~3% duty cycle)

- **Proposed geometry:**
  - 3 x double sided ladders
    - Optimize material budget / alignment.

- **2 designs:**
  - Double sided inner ladders:
    - Priority to r.o. speed & spatial resolution
    - 2 faces: resolution / speed (elongated pixels)
    - Pitch 16x16\(\mu m^2\)/ 16x64\(\mu m^2\) + binary charge encoding
    - \(t_{\text{read-out}} \sim 50\mu s/10\mu s\); \(\sigma_{\text{res}} \sim 3\mu m/6\mu m\)
    - 2012: Mimosa-30 prototype (AMS 0.35 \(\mu m\))
      with 2 sided read-out
  - Outer ladders: power dissipation
    - Minimize \(P_{\text{diss}}\) while keeping good spatial resolution
    - Pitch \(\sim 35x35\ \mu m^2\) + ADC 3-4 bits
    - \(t_{\text{read-out}} \sim 100\ \mu s\)
    - 2012: Mimosa-31 prototype (AMS 0.35 \(\mu m\))
      with 4-bit ADC
Toward new applications
Upgrade for more demanding applications

- CPS are also considered by forthcoming projects
  - CBM @ FAIR (>2016): baseline
  - ILD @ ILC@ 500 GeV: TDR option
  - ALICE @ LHC: baseline for ITS upgrade

<table>
<thead>
<tr>
<th></th>
<th>$\sigma_{\text{single point}}$</th>
<th>read-out time</th>
<th>TID</th>
<th>Fluence $n_0$/cm$^2$</th>
<th>$T_{\text{coolant}}$ °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>5 µm</td>
<td>~200 µs</td>
<td>150 kRad</td>
<td>$3 \times 10^{12}$</td>
<td>30</td>
</tr>
<tr>
<td>future projects</td>
<td>3-5 µm</td>
<td>1-30 µs</td>
<td>up to 10 MRad</td>
<td>up to $10^{14}$</td>
<td>&lt; 0 - 30</td>
</tr>
</tbody>
</table>

⇒ higher particles rates

- ILC motivations
  - Robustness with respect to predicted beam background ⇒ occupancy
  - Capabilities to stand the increased occupancy @ 1 TeV (x3-5)
  - Stand alone tracking capabilities (low momentum tracks)

- How to improve read-out speed?
  - Elongated pixels (+staggered pixels)
    - Less row per column
    - Allow in pixel discriminator ⇒ r.o $\geq$ 2 x faster
  - More parallelisation
    - 2 or 4 rows read out simultaneously ⇒ r.o $\geq$ 2-4 x faster
    - Sub arrays read out in // ⇒ r.o $\geq$ 2-4 x faster
    - Only possible in smaller feature size process (0.18 µm) see next slide
Evolving to an optimal process: Tower-Jazz 0.18 μm

• CMOS 0.35μm process does not allow to fully exploit the potential of CPS

• Main limitations of 0.35μm:
  - Feature size ⇒ in pixel circuitry, r.o. speed, power consumption, radiation hardness
  - Number of metal layers ⇒ in pixel circuitry, r.o. speed, insensitive area
  - Clock frequency ⇒ data output
  - Epitaxial layer flexibility: (thickness and resistivity) ⇒ Charge collection/sharing

• Tower-Jazz 0.18 μm
  - Smaller feature size process
  - Stitching ⇒ multi chips slabs (yield ?)
  - 6 metal layers ⇒ in pixel discrim.
  - Deep P-well ⇒ small pitch in pixel discrim.
  - higher epitaxial resistivity (1-6 kΩ.cm), epi thickness 18-40 μm
    ⇒ Enhances signal
    ⇒ Higher read-out speed, higher radiation tolerance
    ⇒ Faster and smarter pixels
Validation of the 0.18μm technology roadmap

- **Goal:** ALICE ITS upgrade (cf. TDR draft) ⇒ scheduled for 2017-18 LHC shutdown
  - Additional L0(22mm) + replacement of inner layers
  - Scheduled for 2017-18 LHC long shutdown
    - (See talks by Beolè and Bufalino)
    - 0.25-1 MRad + 0.3-1x10^{13} n_{eq}/cm^2
    - Chip sensitive area 1x3 cm^2
    - Inner layers ⇒ 0.3% X0
    - Spatial resolution ~ 4 μm
    - Read-out speed ~ 10-30 μs

- **STEP 1 (2012): First prototypes** ⇒ Validation of MIP detection performances

- **STEP 2 (2013):**

- **STEP 3 (2014-15):** 2 strategies
  - **MI STRAL**
    - Col. // read-out with in pixel ampli.
    - Simultaneous 2 rows encoding (x2 faster)
    - Read-out speed ~ 30 μs
  - **ASTRAL**
    - In pixel discri & 2/4-row encoding
    - 2-4 x faster than M22THR ⇒ r.o. speed ~ 10-20 μs
    - P_{diss} ~< 150-200 mW / cm^2
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    - Spatial resolution ∼ 4 µm
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    - P_{diss} ∼< 150-200 mW / cm^2

- Engineering run Tower 0.18 µm
  - Read-out architecture
    - Mimosa-22THRA1/A2 (1l)
    - Mimosa-22THR (2l)
    - (next slides)
  - Pixels architecture
    - Noise: Mimosa-32N1/N2
    - Optimisation Mimosa-32FEE
    - Pixels/diodes dim.: Mimosa-34
  - Charge encoding
    - AROM-0 (1bit)
    - MI MADC (3bits)
  - Sparsification
    - SUZE-02
    - (next slides)

14th ICATPP Conference, 2013
Auguste Besson
STEP 1: Tower-Jazz 0.18 µm

- 2012: First prototypes (M32 & M32ter)
  - Validation of MIP detection performances (120 GeV/c Pions @ CERN)
    - Charge collection properties, pitch, in pixel amplification, CDS, etc.
    - Beam test: SNR & det.eff. 20 µm pitch (1MRad, $10^{13}$ n$_{eq}$/cm$^2$ @ 30 °C)
  - Remaining room for improvement
    - Suspected RTS noise
STEP 1: Resolution with digital output

- Resolution obtained from analog data + simulated binary charge encoding
  - Spatial resolution vs discriminator threshold scan

<table>
<thead>
<tr>
<th>Pixel Dim. [$\mu m^2$]</th>
<th>20 x 20</th>
<th>22 x 33</th>
<th>20 x 40</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{sp}^{bin}$ [$\mu m$]</td>
<td>3.2 ± 0.1</td>
<td>5.1 ± 0.5</td>
<td>5.4 ± 0.1</td>
</tr>
</tbody>
</table>

← expect ~ 2.8 $\mu m$ for 17 x 17 $\mu m^2$ pixels (ILD-DBD)
STEP2: Read-out architecture ⇒ M22 THRA1 results

• MIMOSA-22THRA1 design (adapted from M28-STAR)
  - 128 col. x 320 rows (22x22/33 \(\mu\)m\(^2\))
    ➢ + end of col. discr
  - 8 col. with analog output for tests
  - Rolling shutter (single row) read-out
    ➢ \(t_{r.o.} \sim 50\ \mu\)s
  - RTS noise optimisation:
    ➢ enlarged preamp T gate
  - 4 different submatrices
    ➢ Study RTS
  - Different epitaxial layers
    ➢ 18\(\mu\)m(HR18), 20\(\mu\)m(HR20), etc.

• Beam Test (5GeV e\(^-\) @ DESY)
  - Det.Eff. \(\geq\sim 99.5\ %\) with fake \(\leq 10^{-5}\) (lab test)
    ➢ Few \(10^{-3}\) inefficiency may come from track-hit mismatch (under investigation)
M22 THRA1 results: digital part

- Fixing the Noise tail
  - Enlarge pre-amp transistor gate dimension
    - Right: L/W = 0.18/1 μm → Tail
    - Left: L/W = 0.36/1 μm
    - TN ~ 17 e^-

- Efficiency - fake rate
  - vs discr threshold scan
  - Different epitaxial layers thicknesses
    - 18 μm (HR18), HR20, HR30
M22 THRA1 results: analog part (S2)

- Analog part of M22 THRA1 → HR18 @ 30°C:
  - SNR of cluster seed pixel ~ 34 (in agreement with M32ter values)
Step 2: Pixel optimization ⇒ M34 results

- Mimosa 34: explores various pixel dimensions (pitch, diode, etc.)
  - Different epitaxial layer thickness 18μm (HR18), 20μm (HR20)
  - Signa-to-Noise ratio distribution
  - e.g. 22x33 μm² (2T) pixels @ 30 °C
    ⇒ ~0.1% of cluster with SNR <8

⇒ diode size optimisation ⇒ 8 μm² preferred
**Summary**

- CPS have reached a level of maturity which allow them to equip vertex detector of HEP experiments whose specifications are governed by:
  - Spatial resolution, material budget, power dissipation and costs.
  - 0.35 μm technology already suited for STAR-PXL, ILC@ 500 GeV, etc.

- 0.18 μm technology will allow to exploit fully the potential of the technology
  - Promising results on first prototypes
  - More demanding applications are now possible
    - Faster read-out O(few μs), enhanced rad. tol. O(10^{14} n_{eq}/cm^2 + 10MRad @ 30°C)
    - ILC @ 1 TeV, ALICE-ITS upgrade, CBM@ FAIR, ALDA beam telescope, etc.

- 0.18 μm roadmap
  - 2013: validation of upstream and downstream sensor elements
  - 2014-15: validation of complete sensor architecture (1cm^2 ASTRAL/MISTRAL proto)
  - 2015-16: preproduction of ASTRAL/MISTRAL sensors ⇒ CBM, ALICE
  - 2017-19: adapt MISTRAL/ASTRAL for ILC-VTX detector
Back up
Applications of CPS : ALICE-ITS Upgrade

- ITS upgrade: scheduled for "2017-18" LHC long shutdown
  - see talk of M. Sitta
  - exploits space left by replacement of beam pipe
    with small radius (19 mm) section
  - addition of L0 at \( \sim 22 \) mm radius to present ITS
    & replacement of (at least) inner part of present ITS
  - 1st tracker entirely composed of pixel sensors:
    - 7 layers with pixels: \( \gtrsim 9 \text{ m}^2 \), \( O(10^{10}) \) pixels!
    - material budget of inner layers \( \sim 0.3 \% X_0 \)

- Differences w.r.t. ULTIMATE/MIMOSA-28:
  - \( \sim 0.25/1 \) Mrad & \( 0.3/1 \cdot 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2 \) at \( T = 30^\circ\text{C} \) (target values)
  - \( 0.18 \ \mu m \) 4-well HR-epi techno. (Instead of \( 0.35 \ \mu m \) 2-well hR-epi)
  - \( \sim 1 \times 3 \text{ cm}^2 \) large sensitive area (instead of \( 2 \times 2 \text{ cm}^2 \))
  - parallelised rolling-shutter (pot. in-pixel discri.) \( \Rightarrow \sim 10-30 \ \mu s \)
  - 1 or 2 output pairs at \( \gtrsim 300 \text{ MHz} \) (instead of 1 output pair at 160 MHz)
  - \( \sigma_{sp} \sim 4 \ \mu m \); ladders \( \sim 0.3 \% X_0 \)

 الفني

- CDR approved by LHCC in Sept. 2012 \( \Rightarrow \) TDR Draft-1 close to release
- 2 alternative sensors developed at IPHC: MISTRAL (end-of-col discri) & ASTRAL (in-pixel discri)
## 0.35 μm limitations

<table>
<thead>
<tr>
<th>CMOS process fab. parameters</th>
<th>In-pixel circuitry</th>
<th>Read-out speed</th>
<th>Power consum.</th>
<th>Insensitive areas</th>
<th>TID (&gt; ILC)</th>
<th>Data throughput</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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<tr>
<td>Planar techno.</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nb (metal layers)</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Expt-System</th>
<th>$\sigma_t$</th>
<th>$\sigma_{sp}$</th>
<th>TID</th>
<th>Fluence</th>
<th>$T_{op}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>$\lesssim 200 \mu s$</td>
<td>$\sim 5 \mu m$</td>
<td>150 kRad</td>
<td>$3 \cdot 10^{12} \text{ n}_{eq}/\text{cm}^2$</td>
<td>$30^\circ \text{C}$</td>
</tr>
<tr>
<td>ALICE-ITS</td>
<td>10-30 $\mu s$</td>
<td>$\sim 5 \mu m$</td>
<td>700 kRad</td>
<td>$10^{13} \text{ n}_{eq}/\text{cm}^2$</td>
<td>$30^\circ \text{C}$</td>
</tr>
<tr>
<td>CBM-MVD</td>
<td>10-30 $\mu s$</td>
<td>$\sim 5 \mu m$</td>
<td>$\lesssim 10 \text{ MRad}$</td>
<td>$\lesssim 10^{14} \text{ n}_{eq}/\text{cm}^2$</td>
<td>$\ll 0^\circ \text{C}$</td>
</tr>
<tr>
<td>ILD-VXD</td>
<td>$\lesssim 10 \mu s$</td>
<td>$\lesssim 3 \mu m$</td>
<td>O(100) kRad</td>
<td>O(10$^{11}$) $\text{ n}_{eq}/\text{cm}^2$</td>
<td>$\lesssim 30^\circ \text{C}$</td>
</tr>
<tr>
<td>SuperB-SVT</td>
<td>$\lesssim 2 \mu s$</td>
<td>$\sim 10 \mu m$</td>
<td>5 MRad/yr $\times$ SF</td>
<td>$5 \cdot 10^{12} \text{ n}_{eq}/\text{cm}^2/\text{yr} \times$ SF</td>
<td>$\lesssim 10^\circ \text{C}$</td>
</tr>
</tbody>
</table>
FPN of 2-row r.o. (2 discr./col.):

- concern: analog/digital signals coupling \( \Rightarrow \) FPN
- Measured FPN (dblle-row) \( \lesssim 5 \text{ e}^- \text{ENC} \)
  \( \Rightarrow \) FPN (sngle-row) \( \lesssim 3 \text{ e}^- \text{ENC} \)
  \( \Rightarrow \) Marginal noise increase
Deep P-well
MI STRAL
HR 18 vs HR 20

MIMOSA 34, Signal/Noise

Pixel 22x33 μm² diode 11 μm at $T_{cool} = 30°C$

- epi. HR 18 μm, MPV = 43.6 ± 0.5
- epi. HR 20 μm, MPV = 44.9 ± 0.1