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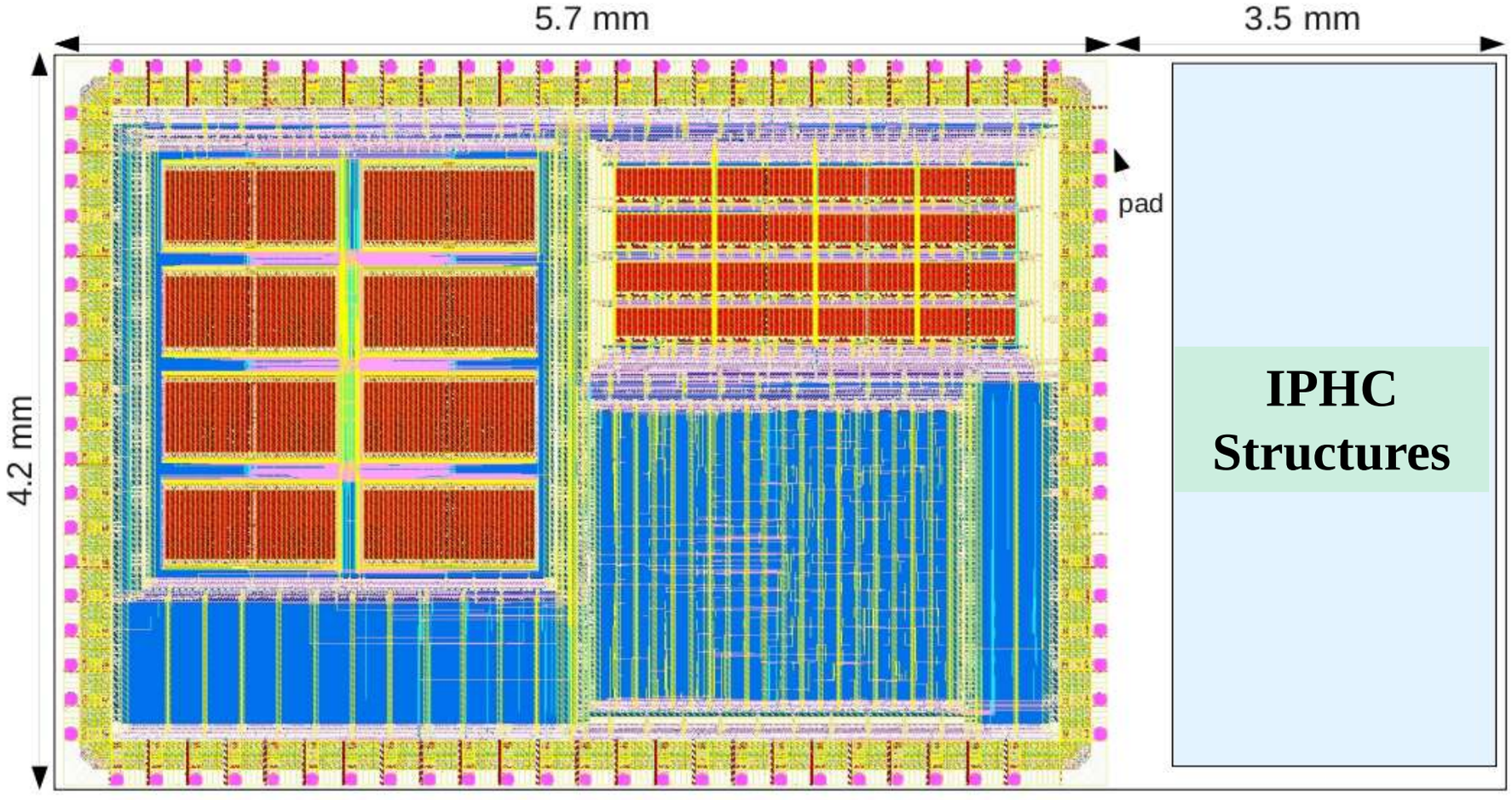
Mimosa 32 mini

Tower 0.18 um
SEU test chip

Pad size 57 um x 57 um

Long side pitch: 211.46 um

Short side pitch: 194.43 um



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Mimosa32bis: Tower CIS, February 2012 submission: 4 Metal, MiM Capacitor, Quadruple Well (deep-N and deep-P wells), std epi 18 SF arrays

Address decoding:

A0 . . . . . A8

A16 . . . . . A24

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M32 bis SF structures:

- P1 2T_ELT_11u (M32_P1)
- P2 3T_ELT_11u (M32_P2)
- P101 3T_ELT_9u
- P102 3T_ELT_16u
- P103 3T_ELT_3u
- P104 3T_ELT_9u_FullDPW_o6u
- P105 3T_ELT_3u_FullDPW_o6u
- P106 3T_ELT_9u_activA
- P107 3T_ELT_9u_activB
- P108 3T_ELT_9u_Gox_0V
- P109 3T_ELT_9u_Gox_floating
- P110 3T-ELT-NoDiode!
- P111 3T_ELT_9u_HalfPinnedA
- P112 3T_ELT_9u_HalfPinnedB
- P113 3T_ELT_9u_HalfPinned_NwellA
- P114 3T_ELT_9u_HalfPinned_NwellB
- P115 3T_ELT_20u_AC
- P116 3T_ELT_20u_AC_NoPwell

All transistors: hVt (ll) !

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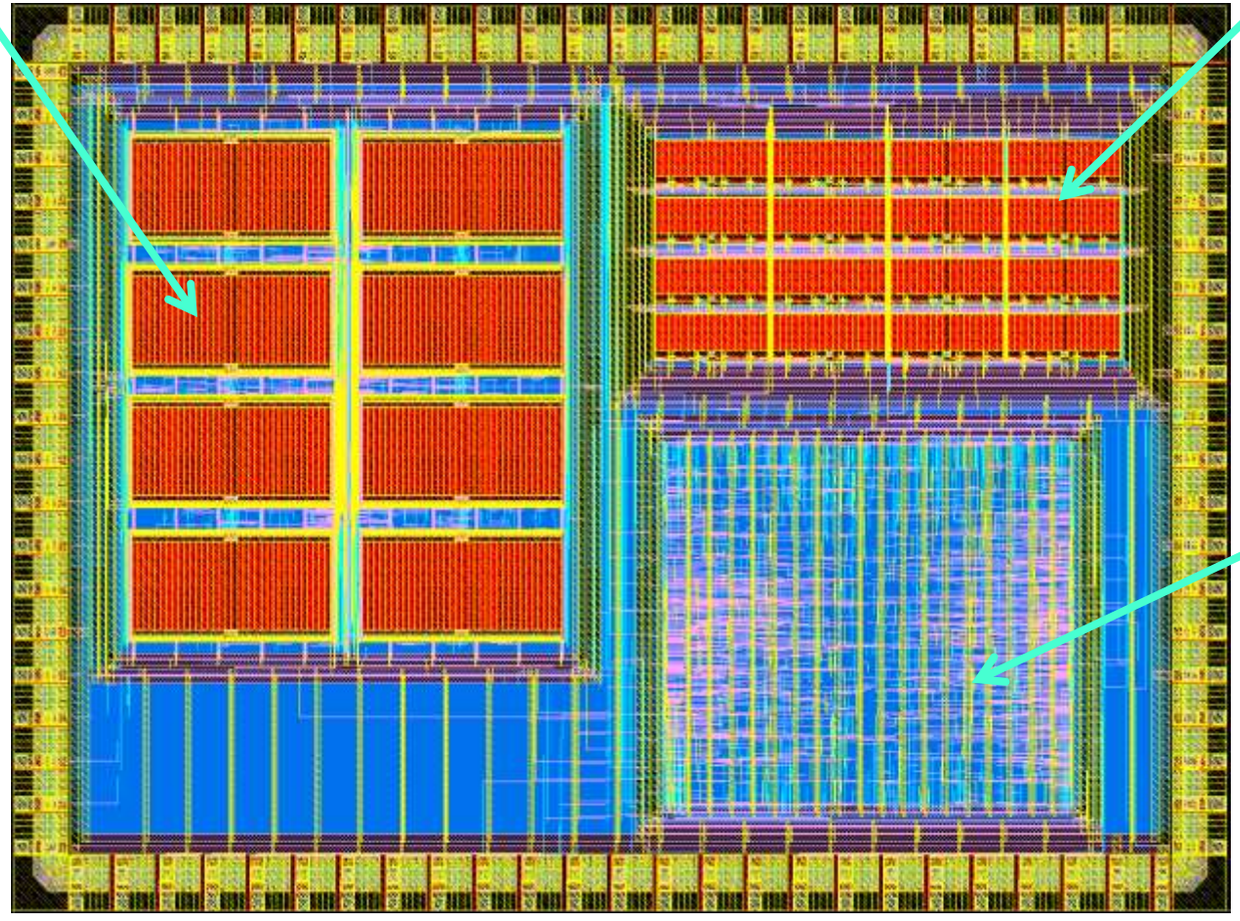
SEU CHIP Layout

Double Port RAM 32kbit 2048@16 bits)

Single Port RAM 16kbit 1024@16 bits



Shift register 32768 Flip_Flop