**MIMOSA VI**

**Pixel design features**
- only NMOS transistors, nwell/psub and pdiff/nwell diodes and poly1-to-poly2 capacitors.

**MIMOSA VI design features**
- 0.35 μm CMOS 4.2 μm thick EPI layer,
- 1 array (24+6) × 128 pixels, pitch 28 × 28 μm²,
- 24 columns read-out in parallel,
- 30MHz f_clk, 6 clock cycles per pixel,
- amplification and double sampling operation on-pixel,
- discrimination integrated on chip periphery,
- diode (nwell/p-epi) size 4.0 × 3.7 μm² - 3.5 fF,

MIMOSA VI chip layout (IREs-LEPSI/DAPNIA collaboration)