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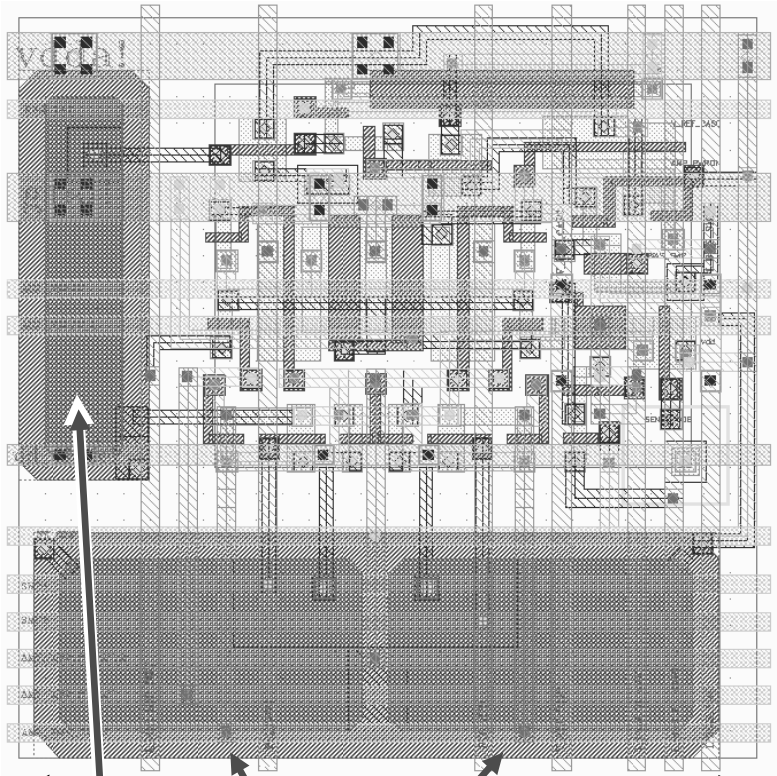
☑ MIMOSA VI

Pixel layout



◎ Pixel design features

- only NMOS transistors, nwell/psub and pdiff/nwell diodes and poly1-to-poly2 capacitors.

◎ MIMOSA VI design features

- 0.35 µm CMOS 4.2 µm thick EPI layer,
- 1 array (24+6) × 128 pixels, pitch 28 × 28 µm^2,
- 24 columns read-out in parallel,
- 30MHz f_{clk}, 6 clock cycles per pixel,
- amplification and double sampling operation on-pixel,
- discrimination integrated on chip periphery,
- diode (nwell/p-epi) size 4.0 × 3.7 µm^2 - 3.5 fF,

MIMOSA VI chip layout (IReS-LEPSI/DAPNIA collaboration)