MIMOSA-24 — sensor description

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1 Motivation for MIMOSA-24 production

The XFAB 0.35μm process was an interesting option for building the sensors for particle tracking. The investigation of performances of this process was motivated by the fact, that the XFAB foundry announced an upcoming 0.35μm process based on a high resistive EPI layer. As it was shown in section **??**, the performance of MIMOSA-25 chip after neutron irradiation was a mile stone in the MAPS development. However, the MIMOSA-25 process featured a relatively large feature size. The XFAB 0.35μm technology, based on the high resistive EPI layer, would open the possibility for production of sensors equipped with a signal processing, but more robust to the non-ionizing radiation. The remaining questions are related to the 0.35μm XFAB process quality and its radiation hardness, as compared to the AMS-OPTO one.

2 The first prototype in the XFAB 0.35 μm technology – MIMOSA-24

The array of MIMOSA-24 was divided in four parts equipped with its own analogue outputs. Each of such sub-arrays had a so called ”test row”, where the sensing diode was disconnected from the source follower. The purpose of the ”test row” was to allow for the gain calibration of each output. In addition, each from the four mentioned sub-arrays was additionally divided in two parts containing different pixel designs. As a consequence, eight sub-arrays was implemented inside the sensor. Table 1 and Fig.1 contains details related to all sub-arrays. The implemented diodes featured the size of 4.3×3.4μm^2, 5.0×5.0μm^2 and 6.0×6.0μm^2. The pixels were enclosed in the pitch size of 20 μm and 30 μm.

In order to improve the radiation hardness to the ionizing radiation, two radiation tolerant diodes were implemented. They were named RadTol$_{AMS}$ and RadTol$_{ELT}$. The design of RadTol$_{AMS}$ diode was supposed to follow the radiation tolerant diode design developed with the AMS technology. The idea of the AMS design was to break the path for the leakage current, induced by ionizing radiation, by impelemntation of the thin oxide around the sensing diode. However, due to the different design rules, as compared AMS technology, the reproduction of such radiation hard diode in the XFAB process was difficult. Finally, the thin gate oxide surrounding the n-well diode does not extend up to the n-well – p-EPI boundary, as it was in the case of AMS. The RadTol$_{AMS}$ diode design is shown in in Fig.3(b), and it can be compared to the standard, not radiation tolerant diode from Fig.3(a). The second radiation tolerant diode RadTol$_{ELT}$, shown in Fig.3(c), used the ELT in order to implement the thin gate oxide around the diode. In case of this design, the sensong diode was build-in the n-type ELT. Also, in this case the diode design is different form the AMS one. Again the thin oxide does not cover the n-well – p-EPI boundary, and moreover, it is placed in a distance of 0.6 μm from the sensing diode. Hoverer, the implemented thin oxide is suppose to break the leakage current path formed after ionizing radiation, and as a consequence limit the diode leakage current.

Table 1: *MIMOSA-24 – the main features of implemented pixels.*

Matrix	Diode size	Pitch	Sub-array size	Description
0	$4.3{\times}3.4\mu m^2$	$20\mu m$	$31{\times}32$	Self Biased diode
1	$6.0{\times}6.0\mu m^2$	$20\mu m$	$32{\times}32$	Self Biased diode
2	$4.3{\times}3.4\mu m^2$	$20\mu m$	$31{\times}32$	3T with reset
3	$6.0{\times}6.0\mu m^2$	$20\mu m$	$32{\times}32$	3T with reset
4	$4.3{\times}3.4\mu m^2$	$20\mu m$	$31{\times}32$	$RadTol_{ELT}$, 3T with reset
5	$4.3{\times}3.4\mu m^2$	$20\mu m$	$31{\times}32$	$RadTol_{AMS}$, 3T with reset
6	$4.3{\times}3.4\mu m^2$	$30\mu m$	$15{\times}32$	3T with reset
7	$5.0{\times}5.0\mu m^2$	$30\mu m$	$16{\times}32$	3T with reset

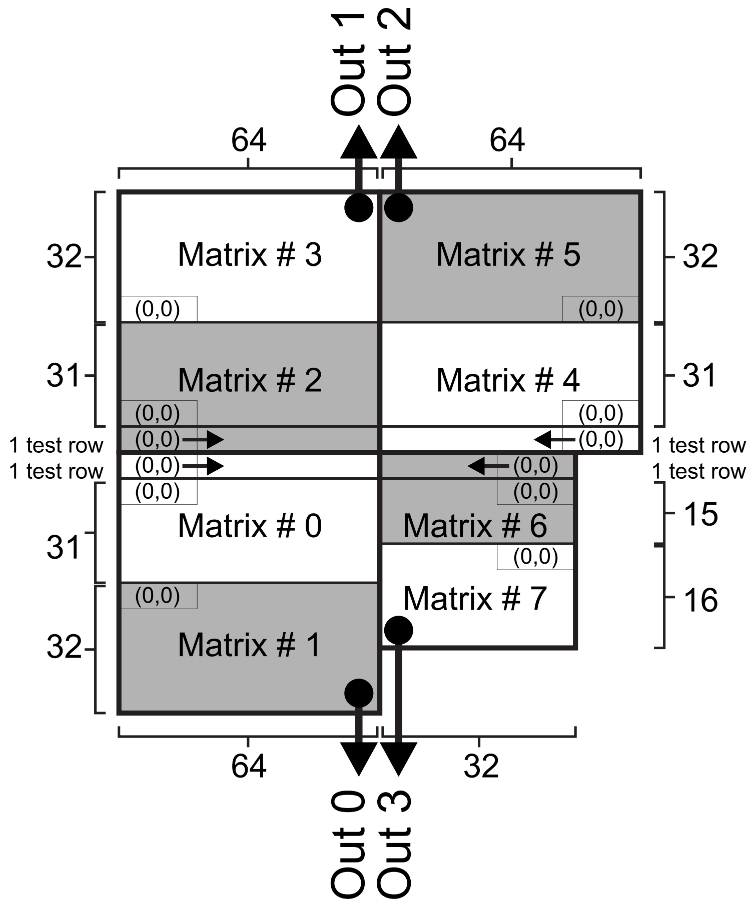


Figure 1: *MIMOSA-24 – matrix organization. (0,0) states for the first read-out pixels.*

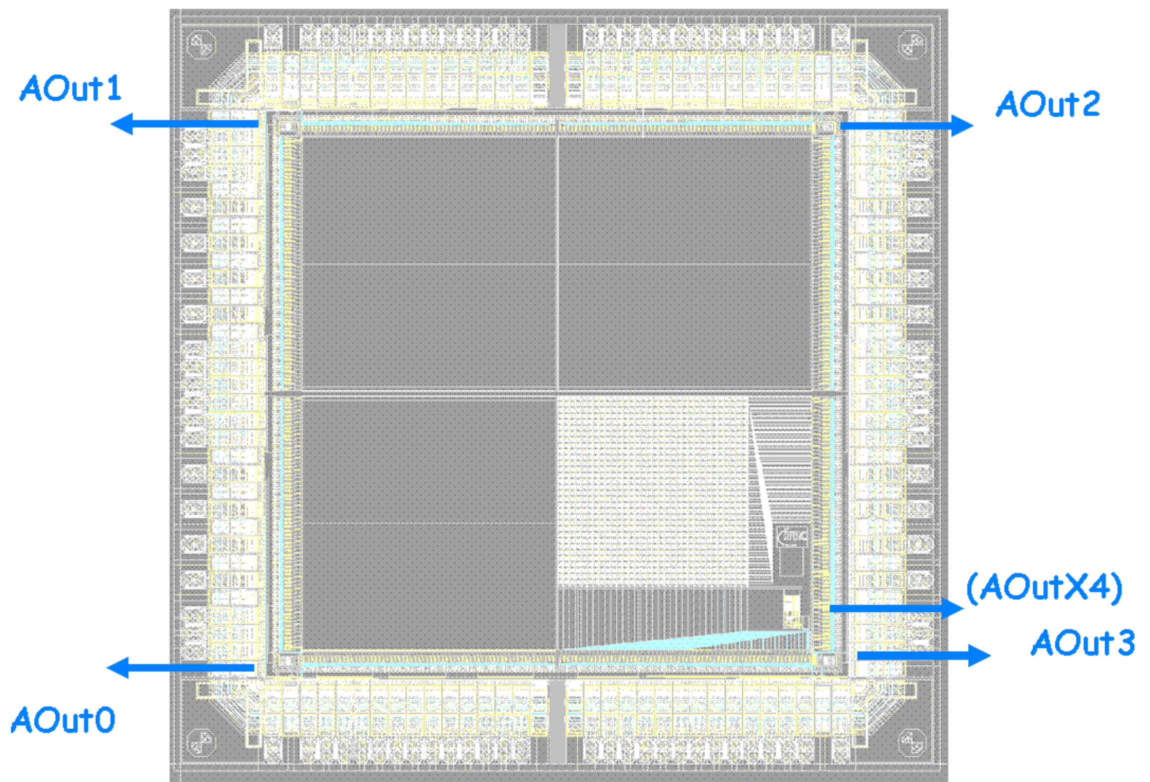
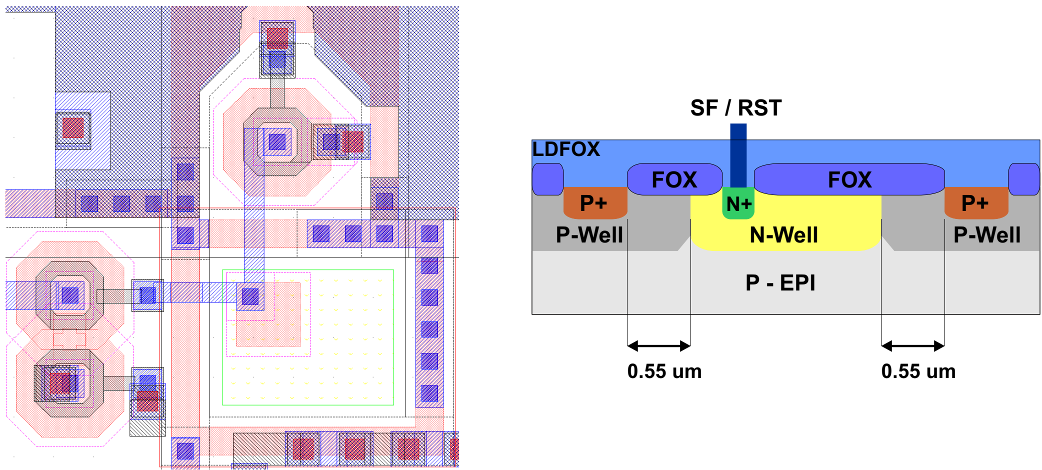
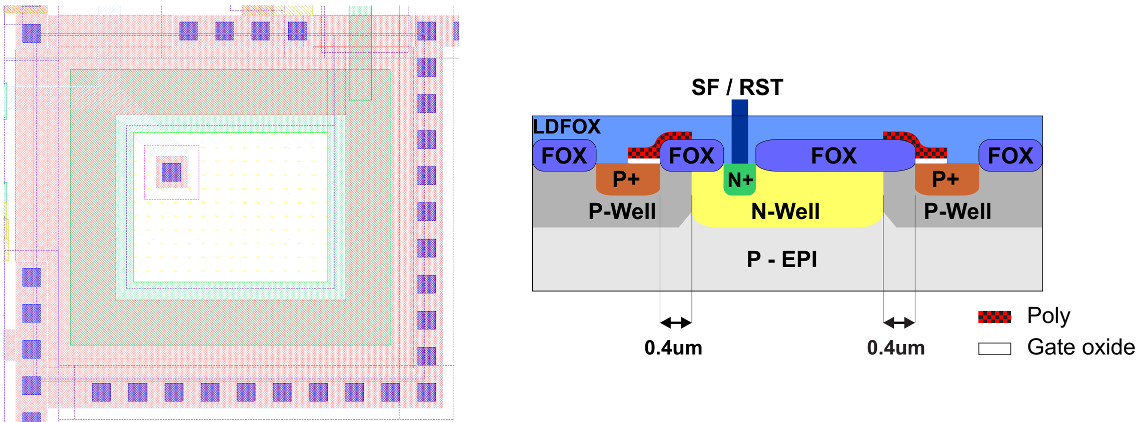


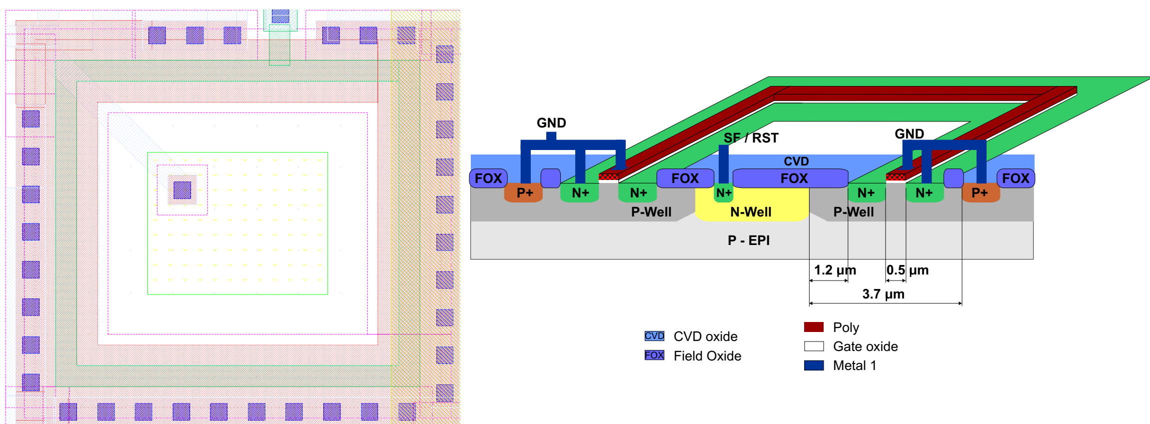
Figure 2:
MIMOSA-24 – sensor layout.



(a) standard diode with p+ guardring



(b) radiation tolerant diode based on the design tested with the 0.35μm AMS-OPTO technology



(c) radiation tolerant diode based on the enclosed layout transistor

Figure 3: *Diode implemented inside MIMOSA-24 prototype.*

3 Sensor gain calibration and pixel capacitance measurements

The sensor calibration with an ^{55}Fe source was performed for all devices under test. The calibration procedure followed the one described in section **??**. In addition, the four ”test rows” of MIMOSA-24 were used to estimate the pixel capacitance. The ”test rows” contained pixels where the output signal was not provided by the sensing diode. Instead, the sensing diode was bypassed, and the signal came from the reset transistors, as it is shown in Fig.4. When *Reset* was active, the *Vdiode* voltage was propagated directly to the source follower input gate.

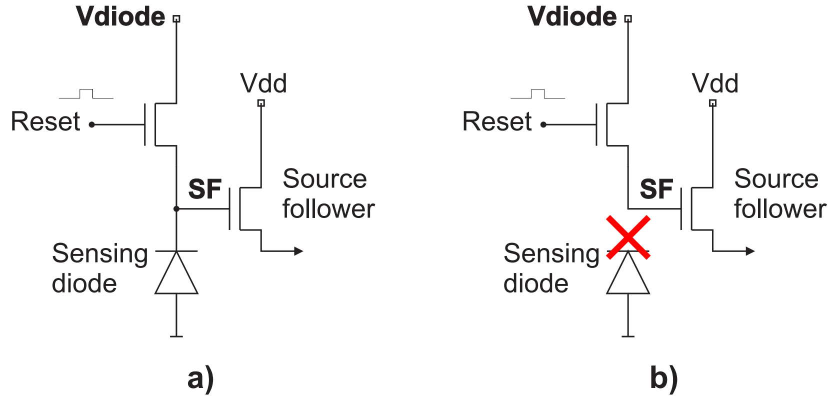


Figure 4: *The standard row (a) and the test row (b) of the MIMOSA-24 prototype*

The pixel capacitance has several components. The main ones are the sensing diode capacitance, the parasitic capacitance of the source follower and the reset transistor. In order to estimate the pixel capacitances, the following equation was used:

$$Cpx = \frac{Q \cdot q}{V} \tag{1}$$

where Q is the collected charge, V is the corresponding voltage and q states for the electron charge. The value of the charge Q collected in the sensing diode is obtained form the ^{55}Fe peak corresponding to the 5.9 keV. The peaks visible in the ^{55}Fe spectrum corresponds to 5.9 keV and 6.49 keV photons, which energy was transferred to e-h pairs inside the sensing diode. In order to create an e-h pair in silicon, the energy of 3,6 eV is needed. Thus the 5.9 keV photons form ^{55}Fe source will generate approximately $\sim$1640 e-h pairs. If the photon interaction with silicon volume occurs in the sensing diode, the all generated signal charge is collected by the diode. In this case, the calculated charge Q amounts to around 1640 e^-. The voltage V, corresponding to this charge, can be derived from following equation:

$$V = conv \cdot ^{55} Fe5.9eV peakposition[ADC] \tag{2}$$

where the ^{55}Fe5.9keVpeakposition[ADC] states for an ^{55}Fe 5.9 keV peak position measured in

ADC units [1]. The *conv* factor between the input voltage (*Vdiode*) and corresponding output units (ADC units) is given by:

$$conv = \frac{\Delta Vdiode}{\Delta ADC} \tag{3}$$

The remaining question was related to the conversion factor (*conv*) between a diode voltage and ADC units. Since *Vdiode* was controlled externally, the mentioned conversion factor became measurable.

The measurements of *conv* were performed with the "test rows". The *Vdiode* was changed with small steps of 10 mV (Δ*Vdiode*). The corresponding Δ*ADC* counts were recorded in parallel. The range of 0.3 - 3.3 V was covered by those measurements. Figure 5 displays the Δ*ADC* as a function of the *Vdiode*. It was observed that, for *Vdiode* below 1 V and above 3 V the gain decreased. The conversion factor within the *Vdiode* range of 1÷3 V was more stable and amounted to ~205 ADC/10mV, which corresponded to ~49 μV/ADC. The differences in the conversion factor in the *Vdiode* range of 1÷3 V amounted to around 10%. This value could also be used as the measurement uncertainty of *conv* factor.

This estimated conversion factor was used in order to calculate the sensing diode capacitance according to following equation:

$$Cpx = \frac{Q \cdot q}{V} = \frac{^{55}Fe5.9keV charge[e^{-}] \cdot q}{^{55}Fe5.9keV peak[ADC] \cdot conv} = \frac{1640 \cdot q}{^{55}Fe5.9keV peak[ADC] \cdot 49\mu V/ADC} \tag{4}$$

The estimated values of MIMOSA-24 pixel capacitances are presented in Table 2. The measured values of the pixel capacitances were in the same range, as compared to the ones estimated in the past for the AMS-OPTO 0.35μm process.

The expected sensing diode capacitance *Cd* was be calculated using Table **??** related to the XFAB 0.35 μm process specification. The calculated value of the diode capacitance was used after to extract the parasitic capacitances of the reset transistor and the source follower. For example the sensing diode featuring the size of 4.3×3.4μm^2 is expected to have capacitance of:

$$Cd = 4.3 \times 3.4\mu m^2 \cdot 0.12fF/\mu m^2 + (4.3 + 3.4 + 4.3 + 3.4)\mu m \cdot 0.36fF/\mu \approx 6.6fF \tag{5}$$

In the case of MIMOSA-24 3T pixel, featuring the n-well diodes with the size of 4.3×3.4μm^2, the measured pixel capacitance *Cpx* amounted to ~13 fF. This value was compared to the calculated sensing diode capacitance *Cd* of 6.6 fF. It was observed that, around 50% of *Cpx* had its origin in the resent and source follower parasitic capacitances.

[1] ADC units stated for Analog to Digital Converter units

Table 2: *MIMOSA-24 – estimated sensing diode capacitances.*

Diode type	Diode size	Pitch	Capacitance [fF]
SB	$4.3{\times}3.4\mu m^2$	$20\mu m$	13.0 ± 1.4
SB	$6.0{\times}6.0\mu m^2$	$20\mu m$	18.2 ± 2.0
3T	$4.3{\times}3.4\mu m^2$	$20\mu m$	15.0 ± 1.7
3T	$6.0{\times}6.0\mu m^2$	$20\mu m$	18.5 ± 2.0
3T RadTol$_{ELT}$	$4.3{\times}3.4\mu m^2$	$20\mu m$	14.9 ± 1.6
3T RadTol$_{AMS}$	$4.3{\times}3.4\mu m^2$	$20\mu m$	14.3 ± 1.6
3T	$4.3{\times}3.4\mu m^2$	$30\mu m$	$15.8 \pm 1{,}7$
3T	$5.0{\times}5.0\mu m^2$	$30\mu m$	17.0 ± 1.9

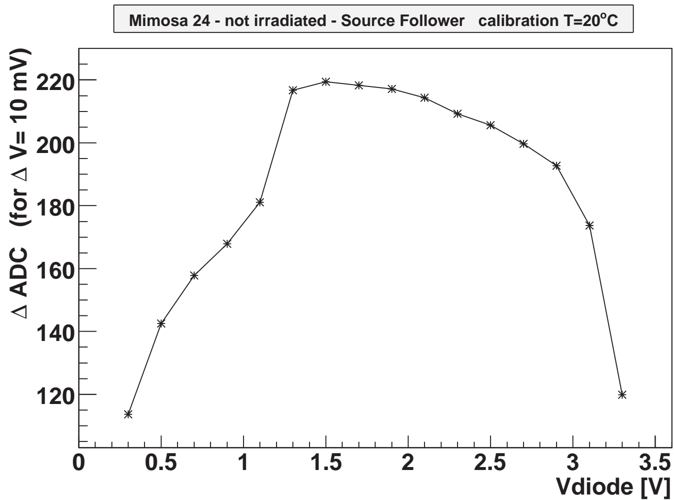


Figure 5: *Gain measurements of MIMOSA-24. ΔADC as a function Vdiode. this plot was obtained with so called "test rows". They allowed for the pixel gain and pixel capacitance measurements*