Wojciech.Dulinski@ires.in2p3.fr

SUZE: the demonstrator of data sparsification circuit for the binary readout MAPS

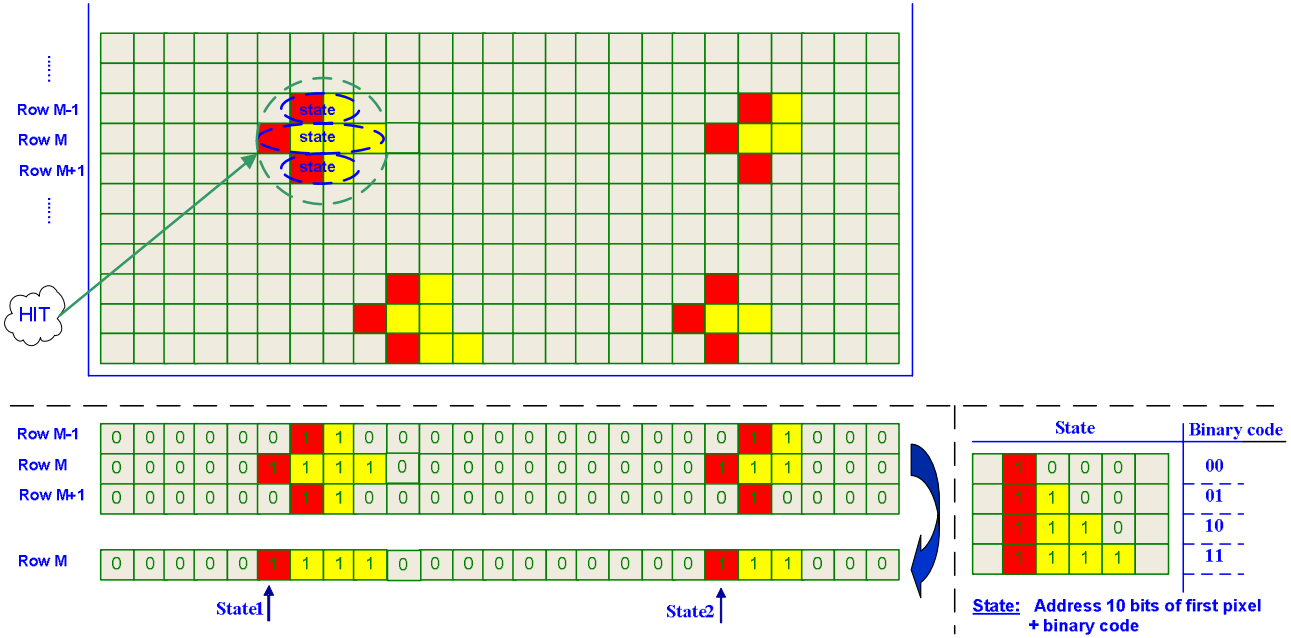
Wojciech Dulinski on behalf of IPHC and SUZE designers: Guy Doziere and Abdelkader Himmi

Outline

- Introduction: hit coding
- SUZE architecture and basic building blocs
- Basic specification and projection for M22+ performance (544 × 1088 pixel tracker)
- Present status of testing
- Conclusions and discussion

Wojciech.Dulinski@ires.in2p3.fr

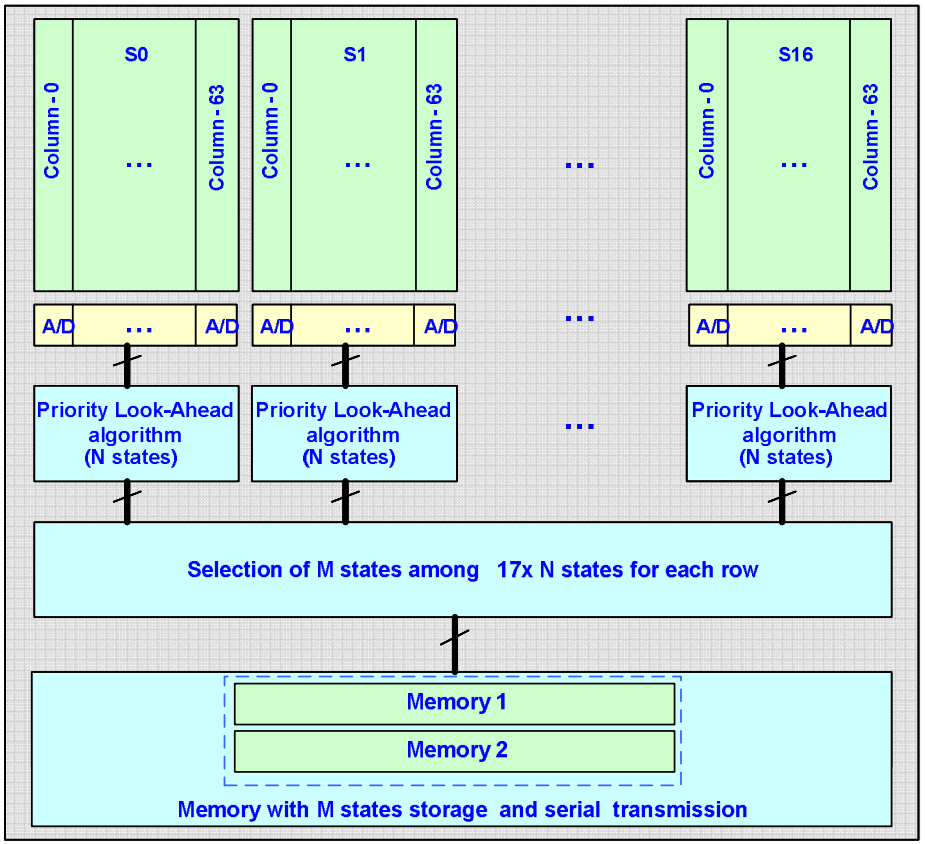
Hit coding proposed for the binary readout MAPS (M22+, MimoSTAR++)



Encoding of adjacent hit pixels in a row (up to four in one group) plus a common row address (if more than one state/row), means data compression but no real clustering.

Wojciech.Dulinski@ires.in2p3.fr

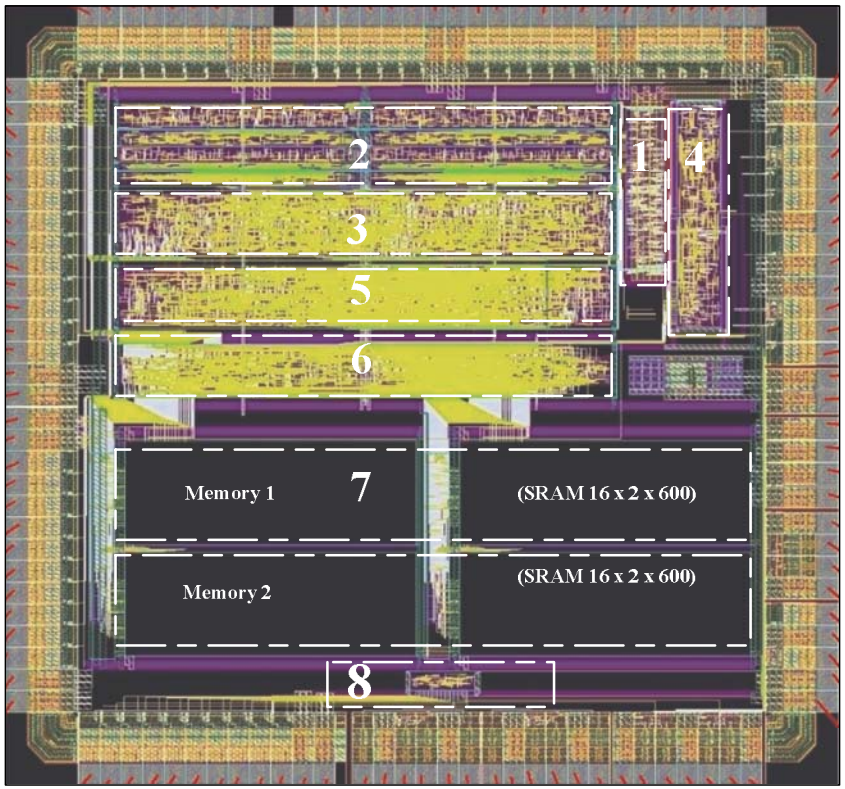
Diagram of M22+ with the basic blocks of sparsifying circuitry



M22+ array size: 1088 x 544 pixels, 18.4 µm pitch (exactly as M22)

Wojciech.Dulinski@ires.in2p3.fr

SUZE: the layout details



Part 1:
JTAG

Part 2:
Priority look Ahead Algorithm

Part 3 and 4:
Sequencer for row, frame and memory synchronization

Part 5:
Selection of 9 states among 2 x 6 states

Part 6 :
Memories management

Part 7 :
FIFO : 2 blocs of memories with M states storage

Part 8 :
Serial transmission

3 × 3 mm²

Wojciech.Dulinski@ires.in2p3.fr

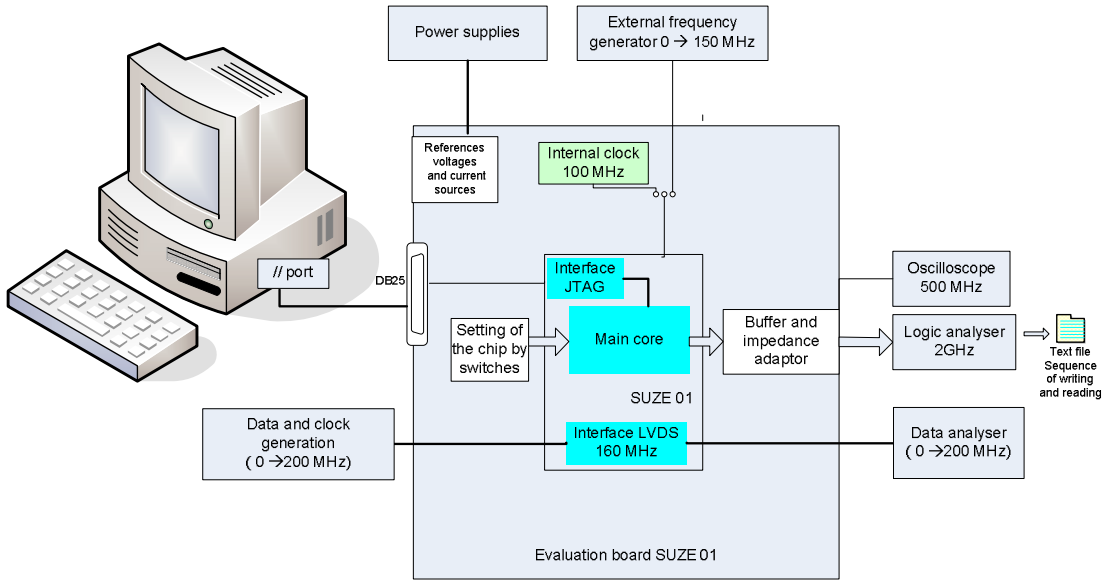
SUZE basic specification and projection for M22+ performance

Part	Parameter	Typical Value	Notes
Oscillator	Frequency	100 MHz	
READOUT	CKRD Frequency	Up to 100 MHz	f_{ck} for the output LVDS
	CKRD Duty Cycle	50%	
JTAG	TCK Frequency	10 MHz	
	TMS Setup/Hold Time	~10 nS	
	TDI Setup/Hold Time	~10 nS	
Memory	sampling frequency	100 MHz	
	size	38400 bits	Organization 600 x 16 x 4
	frequency max	200 MHz	
	Speed of the reading	100 Mbits/s	
States	number of maximum pixels	4	
	address coding	21 bits (10 for row + 11 for column)	
	coding	2 bits	
Bank	number of pixels	64	
	number of states/row	6	
Row	number of banks	2	M22+ : 17
	maximum number of states	9	M22+ : 9
	reading time	160 ns	200 ns
Frame	reading time	≅ 90 µs	M22+ : 110 µs

With present SUZE architecture, the limit for the hit rate is defined by the output data link. For one serial port/chip (1bit wide) @100 MHz, the maximum hit rate is ~300 states/frame (up to 10^6 hits/s; supposing 3 states/hit (overestimation), but beware statistics and the beam structure!). This rate can be (almost) doubled by implementation of two serial links or by running (output port only!) at 200 MHz.

Wojciech.Dulinski@ires.in2p3.fr

SUZE: test bench and present test status



So far, so good: no single bug detected yet. The chip works at the nominal frequency, several different input patterns give the correct sparsified result. More detailed tests in progress.

Wojciech.Dulinski@ires.in2p3.fr

Conclusions

- SUZE under tests, seems to behave according to the design specs

- Proposal for the M22+ output format: one serial link running @100 MHz, providing at least up to ~100 tracks/frame

- Proposal for a common daughter card for M22 and M22+ : see Appendix for the simplified specs

Wojciech.Dulinski@ires.in2p3.fr

Appendix: Aux_PCB for Mimosa22 (digital output)

RG45 connectors, up to 100MHz LVDS

J1 (in): ck, speak, reset (JTAG) , start

J2 (i/o): JTAG (TCK, TDI, TMS, TDO)

J3 (out): ckout, MKsync, MKtest, trg (analog)

J4 (out): ckout, MKsync, MKtest, trg (digital)

J5 – J8: data out (D0 – D15)