MIMOSA11 RADTOL CHIP

- Techno: AMS 0.35 µm OPTO
  - Epi layer = 14 µm
  - 3 metals layers
- 8 sub-matrix, 8 layout variante pixels
  - 1 sub-matrix = 21 x 42 pixels
  - 1 Pixel Pitch = 30 µm x 30 µm
  - Self-bias diode
- Just submitted
# M11 MATRIX

<table>
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<th>ARRAY 0</th>
<th>ARRAY3</th>
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M11 variantes pixels

- ARRAY 1
  - 11) pixel_NWD_SB_GATOX
    - Diode area = 14.62 µm²; RadTol: GATOX ring, dist(n+ poly – NW) = 0; n+ floating, p+ GR, 15 % poly filling
    - n+diff around p+ in the well, spacing = 0.6 µm (min)
  - 12) pixel_REF2_SB_POLY
    - Diode area = 13.44 µm²; Standard diode (the depleted region of the diode intercepts near the surface the LOCOS isolation surface), p+ GR, 15 % poly filling
    - n+diff around p+ in the well, spacing = 0.7 µm

- ARRAY 2
  - 21) pixel_NWD_SB_NPLUS_GATOX
    - Diode area = 14.62 µm²; RadTol: GATOX ring, dist(n+ poly – NW) = 0.15 µm; n+ floating, p+ GR, 15 % poly filling
    - n+diff around p+ in the well, spacing = 0.6 µm
  - 22) pixel_NWELLRING
    - Diode area = 13.44 µm², Standard diode, p+ GR, NW GR (novel idea), p+ GR, 15 % poly filling
    - n+diff around p+ in the well, spacing = 0.7 µm

- ARRAY 0
  - 01) pixel_NWD_SB_DIFF
    - Diode area = 14.62 µm², RadTol: the diffusion layer is used to eliminate the LOCOS oxyde; the p+ GR is put away from the well (0.8 µm), 15 % poly filling
    - n+diff around p+ in the well, spacing = 0.6 µm
  - 02) pixel_REF_SB
    - Diode area= 14.62 µm², Standard diode, p+ GR, NO filling
    - Local n+diff and p+ in the well, spacing = 0.9 µm

- ARRAY 3
  - 31) pixel_NWD_SB_DIFF_GATE
    - Diode area = 14.62 µm², RadTol: undoped diffusion layer in nwell and GATOX ring with poly partially p+doped, dist(poly – NW) = 0, p+ GR, 15 % poly filling
    - n+diff around p+ in the well, spacing = 0.6 µm
  - 32) pixel_REF_SB_POLYGATE
    - Diode area = 14.62 µm², Standard diode, p+ GR, FULL poly filling
    - Local n+diff and p+ in the well, spacing = 0.9 µm