A Fast Architecture Providing Zero Suppressed Digital Output Integrated in a High Resolution CMOS Pixel Sensor for the STAR Vertex Detector and the EUDET beam Telescope

- IRFU & IPHC group -

Outline

- Physics motivation of MAPS (Monolithic Active Pixel Sensors) R&D
- Achieved MAPS performances
- MAPS applications: the STAR vertex detector upgrade & the EUDET beam telescope
- High readout speed, low noise, low power dissipation, highly integrated signal processing architecture
- Conclusion
MAPS: Physics Motivations

- Flavor tagging takes growing importance for understanding the dynamics underlying elementary process in HEP experiments
  - Study short lived particles through their decay vertex

- Vertexing & Tracking:
  - Need excellent reconstruction of secondary vertices
    - Granularity & low material budget
  - Need precise measurement of the momenta of tracks
  - Improve the system’s accuracy by an order of magnitude w.r.t. the state of the art

- Existing pixel technologies are not adequate for this requirement level:
  - CCD (SLD): granular and thin BUT too slow and not radiation hard
  - Hybrid Pixel Sensors (Tevatron, LHC): fast and radiation hard BUT not granular and thin enough

- Aim for an ultra-light, very granular, radiation tolerant, fast and poly-layer vertex detector installed very close to the interaction point
  - Demanding running conditions (occupancy, radiation) !!!

→ MAPS provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power dissipation
Main Features of MAPS

- Metal layers
- Dielectric for insulation and passivation
- Polysilicon
- Radiation
- P-substrate (~100s μm thick)
- Charged particles
- 100% efficiency.

Potential barriers:

$$ V = \frac{kT}{q} \ln \frac{N_{\text{amb}}}{N_{\text{opt}}} $$
MAPS: with Analogue Readout

- ENC ~ 10-15 e-, S/N (MPV) ~ 15-30
  - Detection efficiency > 99.5%, even at operation temperature up to 40°C
- Single point resolution: ~ 1-3 µm for pixel pitches of 10-40 µm

BUT: moderate readout speed for larger sensors with smaller pitch!

- For many applications: high granularity and fast readout required simultaneously
  - Integrating signal processing: ADC, Data sparsification, …

⇒ R&D on high readout speed, low noise, low power dissipation, highly integrated signal processing architecture with radiation tolerance
MAPS Applications

- **STAR Heavy Flavor Tracker (HFT) upgrade**
  - Vertex detector: 2 cylindrical MAPS layers
    - at 2.5 and 7 cm from beam line
  - Vertex development is a 3-step process:
    - 2007: MAPS telescope in STAR environment
      - 3 "MimoStar2" sensors with analogue output
    - 2009: 3 detector sectors, "Phase1" sensors
      - Digital output without zero suppression
      - $t_{int} = 640 \mu s$, (30 μm pitch), ~2x2 cm²
    - 2010: whole detector, "Ultimate" sensors
      - Digital output with integrated zero suppression
      - Faster ($t_{int} \sim 200 \mu s$) and more granular (18.4 μm pitch), ~2x2 cm²

- **EUDET is to provide an infrastructure exploiting detector R&D for the ILC**
  - Construct a 6-MAPS planes beam telescope
    - Extrapolated resolution < 2 μm
  - 2 steps:
    - 2007: demonstrator
      - analog output
    - 2009: final telescope
      - Digital output with zero suppression ($t_{int} \sim 100 \mu s$)
      - Surface: ~1x2 cm²

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Two sensors have similar spec.

- STAR final sensors (Ultimat) spec.:
  - Active surface: ~2x2 cm² (EUDET: ~1x2 cm²)
  - Total ionizing dose: 150-300 kRad per year
  - Non-ionizing radiation dose: charged pions \( \leq O(10^{13}) / \text{year} \)
  - Hit density: \( 10^6 \) hits/s/cm²
  - Readout (integration) time: \( \sim 200 \mu\text{s} \)
  - Power consumption: \( \sim 100 \text{ mW/cm}^2 \)

Design according to 3 issues:

- Increasing S/N at pixel-level
- A to D Conversion at column-level
- Zero suppression at chip edge level

Power v.s. speed:

- Power \( \Rightarrow \) Readout in a rolling shutter mode
- Speed \( \Rightarrow \) 1 row pixels are read out / /

Architecture was validated by 2 prototypes:

- Mimosa22: pixels and A to D conversion
  - 576x128, pixel pitch 18.4 µm
- SUZE: zero suppression
Pixel design:
- Optimize diode size: charge collection, S/N
- Amplification in pixel: improve S/N
- Correlated double sampling (CDS) in 2 levels: pixel, discriminator

- Digital commands common for 1 row
- Up to 1152 pixels per row
- RO: 16 clock cycles per row
- CK: 80-160 MHz
- RO time: 100-200ns/row depending on the size of pixel array
Common Source (CS) amplification in pixel

- Only NMOS transistors can be used

1. CS + Reset

\[ \text{Gain} = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m2} + g_{m3} + g_{d4}} \]

2. Improved CS + Reset

\[ \text{Gain} = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m2} + g_{d3} + g_{d4}} \]

3. Improved CS + Feedback + Self biased

\[ \text{Gain} = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m2} + g_{d3} + g_{d4}} \]

A negative low frequency feedback was introduced to decrease amplification gain variations due to process variations.
In Pixel amplification & Signal Processing (3)

- Measured Mimosa22 pixel (Amp+CDS) performances (20 °C) before irradiation:

<table>
<thead>
<tr>
<th>Pixel types</th>
<th>Diode size (µm²)</th>
<th>CVF* (µV/e⁻)</th>
<th>ENC (e⁻)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS + Reset</td>
<td>1</td>
<td>15.21</td>
<td>57.3</td>
</tr>
<tr>
<td>Improved CS + Reset</td>
<td>2</td>
<td>15.21</td>
<td>57.3</td>
</tr>
<tr>
<td>Improved CS + Feedback + self biased</td>
<td>3</td>
<td>14.62</td>
<td>55.8</td>
</tr>
</tbody>
</table>

- After ionizing irradiation, feedback self-biased structure has the best performances

- Power consumption ~200 µW / pixel
Increasing Radiation Tolerance in Pixel

- Ionizing radiation tolerance:
  - Pixel circuit level:
    - ELT for the transistor connected to the detection diode
  - Diode level:
    - Remove thick oxide surrounding N-well diode by replacing with thin-oxide

- Non-ionizing radiation tolerance:
  - Reducing pixel pitch $\Rightarrow$ pitch $< 20 \, \mu m \Rightarrow 18.4 \, \mu m$
  - Increasing sensing diode size: limited by layout
  - Reducing integration time $\Rightarrow \sim 100-200 \, \mu s$
A/D conversion: Column-level discriminators

- Choice of number of bits depends on the required spatial resolution and on the pixel pitch
  - These applications ➔ 1 bit ➔ discriminator

- Discriminator design considerations:
  - Small input signal ➔ Offset compensated amplifier stage
  - Dim: 16.4 x 430 µm²
  - Conversion time = row read out time (~200 ns)
  - Consumption ~230 µW

- Measurement results of 128 column-level discriminators (Mimosa22):
  - Temporal Noise: 0.35 mV
  - Fixed Pattern Noise (FPN): 0.2 mV
Mimosa22 preliminary test results: Pixels + 128 Discriminators

- Test in lab:
  - Temporal Noise:
    - 0.64 mV $\Rightarrow$ 11.5 e$^-$
  - FPN: 0.22 mV $\Rightarrow$ 3.9 e$^-$

- Beam test with 120 GeV pions at CERN-SPS
  - Threshold $\sim$ 4 mV $\Rightarrow$ 6 $\sigma$ noise

- Efficiency > 99.5%
- Spatial resolution < 4 µm
- Fake rate < $10^{-4}$
Zero Suppression (SUZE)

- Connected to column-level discriminators outputs
- Zero suppression is based on row by row sparse data scan readout and organized in pipeline mode in three stages
  
  1st stage:
  - 1152 columns terminations $\rightarrow$ 18 banks // scan
  - Based on priority look ahead encoding
  - Find up to N states with column addresses per bank

  2nd stage:
  - Read out outcomes of stage 1 in all banks and keep up to M states
  - Add row and bank addresses

  3rd stage:
  - Store outcomes to a memory
  - memory made of 2 IP's buffers $\rightarrow$ continuous RO
    - 1 buffer stores present frame,
      1 buffer is read out previous frame
  - Serial transmission by 1 or 2 LVDS at up to 160 MHz

- SUZE: all critical paths of design pass test
- Power estimation for full size sensor: 135 mW
Floor Plan of a typical final sensor

EUDET final Sensor has half size
Pixel array: 1152 x 576

- Row sequencer: 350 µm wide, due to 4 level metals, placed at right hand side
- Testability: implemented all along the data path
- Sensor is programmable via a boundary scan controller
  - Bias supplies setting
  - Mode setting
Conclusion

- Sensor's architecture suitable for:
  - STAR vertex detector upgrade
  - EUDET beam telescope

- Development of final sensors for both EUDET and STAR is in progress
  - Final sensors for EUDET before end of 2008
  - Ultimate sensors for STAR in 2009

- Readout speed: 10 k frame/s (EUDET)

- Still need to improve power budget for STAR application
- extra
Zero suppression

Pixel array: 576 x 1152 pixels (EUDET)
1024 x 1152 pixels (STAR)

Readout row by row
The row is divided into 18 banks

Analog to digital conversion at the bottom of each column
(Discriminator or ADC)

Zero suppression algorithm:
Find N Hits for each group
Find M Hits for each row
(With N and M determined by pixel array occupancy rate)

Memory witch stores M hits
Memory 0 for frame N
Memory 1 for frame N-1
Serial transmission by LVDS