Status on CMOS sensors

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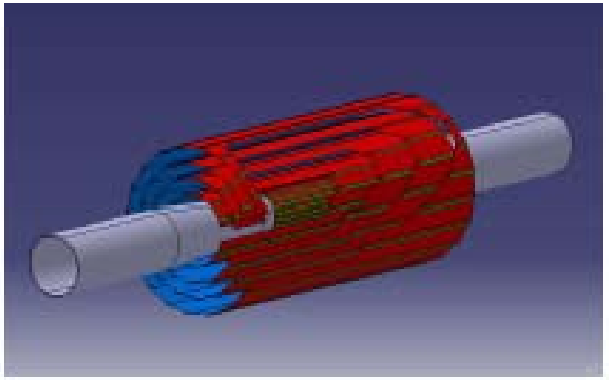
on behalf of
DAPNIA/Saclay, LPSC/Grenoble, LPC/Clermont-F., DESY, Uni. Hamburg, JINR-Dubna & IPHC/Strasbourg
contributions from
IPN/Lyon, Uni. Frankfurt, GSI-Darmstadt, STAR coll.(LBNL, BNL)

- ILC requirements
- Review on CMOS Performances: state of the art
- Progress on fast read-out sensors & ADC
- Roadmap for the coming years
- Summary

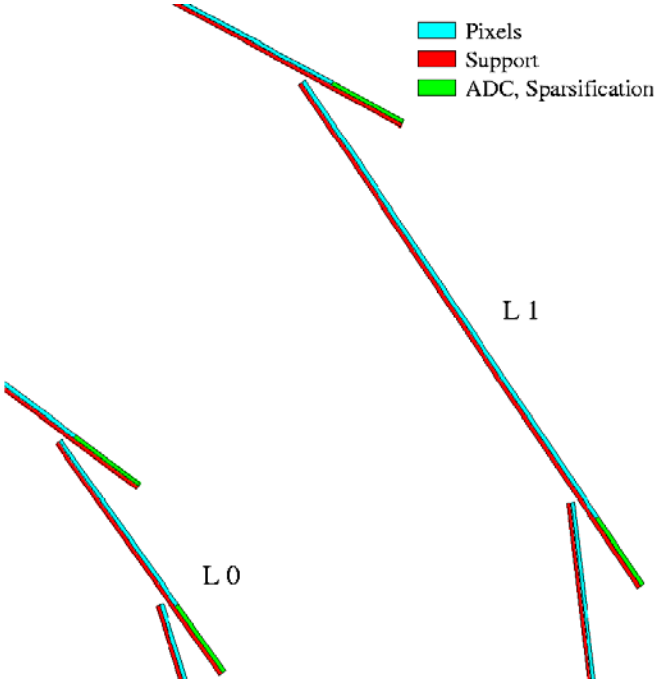
ILC requirements

- Beam background: 1st layer: ≥~ 5 hits/cm^2/BX
  - ➢ (4T, 500 GeV, R_0 = 1.5 cm, no safety factor)
  - – ~ 1.8x10^{12} e$^{\pm}$/cm^2/yr (safety factor of 3)
  - – occupancy:
  - ➢ keep it below ~ few % (cluster multiplicity ~5-10)
  - ➢ aim for a read-out time ~≤ 25 μs



- ILC vertex detector
  - – 5–6 cylindrical layers : ~3000 cm^2
  - – 300-500 million pixels (20–40 μm pitch)
  - – 1st complete ladder prototype ~ 2010

- Read-out speed objectives/ constraints
  - – column parallel read-out ⊥ to beam axis
  - – ADC @ the end of each column
  - – ∅ zero suppression μ-circuits.



Review on CMOS Performances

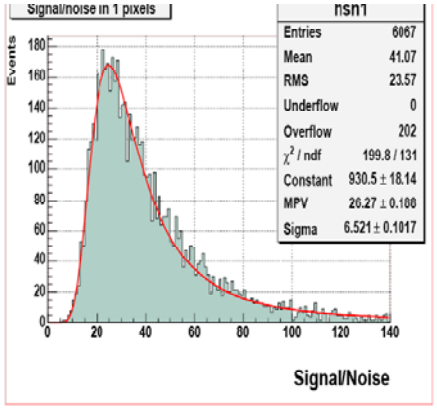
- Detection efficiency
- Radiation hardness
- Resolution

General performances

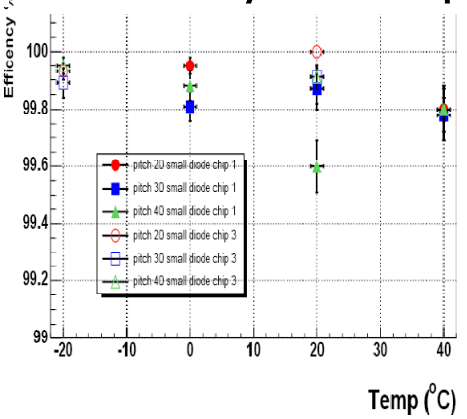
(from H.E. beam tests @ DESY and CERN)

- Charged particle detection well established (analog output)
  - best performing technology:
    - AMS 0.35 µm OPTO
  - N~ 10 e- ⇨S/N (MPV) 20-30
    - eff>~ 99.5 %
  - operating temperature ≥~ 40°C
  - macroscopic sensors:
    - MIMOSA-5 (1 Mpix, 3.5 cm^2)
    - MIMOSA-20 (=M*3) (200 kpix, 1x2 cm^2)
    - MIMOSA-17 (65 kpix, 0.8 x 0.8 cm^2)

S/N (Seed) MPV ~26

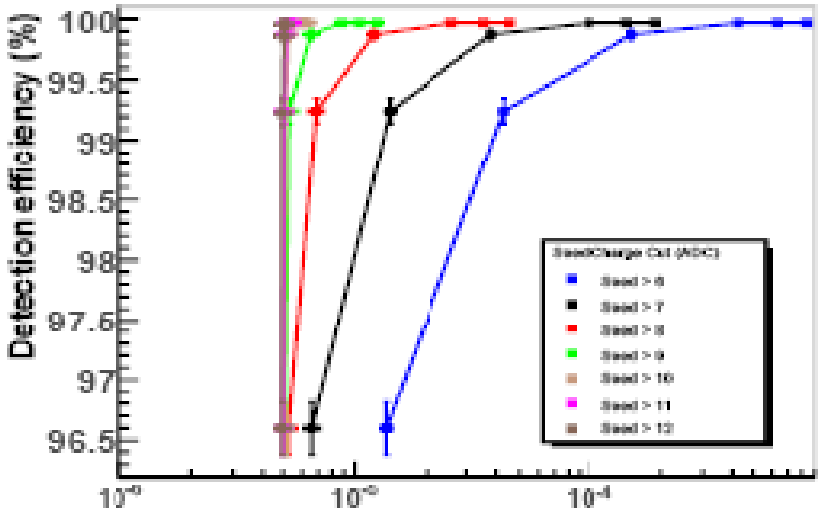


Efficiency vs temp.



- Efficiency vs rate of fake clusters:
  - vary cut on seed pixel:
    - 6 ⇨ 12 ADC units (Noise ~1.5 ADC u.)
  - vary cut on Σ of crown charge:
    - 0,3,4,9,13,17 ADC units
  - eff ~99.9 % for fake rate ~10^{-5}

M9: Efficiency vs fake rate



Radiation hardness: MIMOSA-15

- Non ionising radiation tolerance
  - M-15 irradiated with O(1 MeV) neutrons tested with 6 GeV e- beam (DESY)
    - T = -20 °C, $t_{r.o.}$ ~ 700 µs
    - 5.8x10^{12} n_{eq}/cm^2 values

  derived with standard and soft cuts

Very Preliminary !

Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
S/N (MPV)	27.8 ± 0.5	21.8 ± 0.5	14.7 ± 0.3	« 8.7 ± 2. »	« 7.5 ± 2. »
Det. Eff. (%)	100.	99.9 ± 0.1	99.3 ± 0.2	77. ± 2	84. ± 2.

- Ionising radiation tolerance
  - M-15 irradiated with 10 keV X-rays up to 1 MRad (tested @ DESY)

pixels modified against hole accumulation (thick oxide) and leakage current increase (guard ring)

- T = -20 °C, $t_{r.o.}$ ~ 180 µs
- $t_{r.o.}$ << 1 ms crucial @ room T

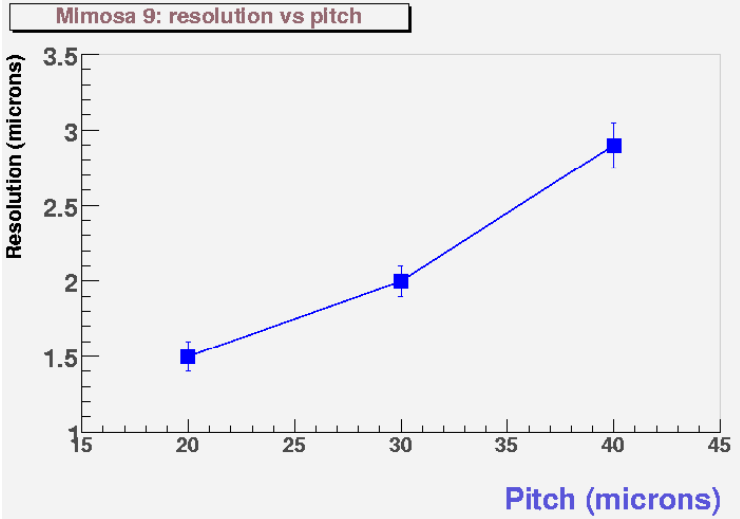
Very Preliminary !

Integ. Dose	Noise	S/N (MPV)	Detection Efficiency
0	9.0 ± 1.1	27.8 ± 0.5	100 %
1 MRad	10.7 ± 0.9	19.5 ± 0.2	99.96 ± 0.04 %

- Preliminary conclusion
  - at least 3 years of running viable @ room T° (or close to)
  - further assessment needed
    - test 10 MeV e^-
    - sensors with integrated CDS, ADC, etc.

Spatial Resolution vs ADC resolution

- Single point resolution vs pitch
  - hit position reconstructed with eta function, exploiting charge sharing between pixels
  - σ_{sp} ~ 1.5 μm (20 μm pitch)
  - obtained with charge encoded on 12 bits.

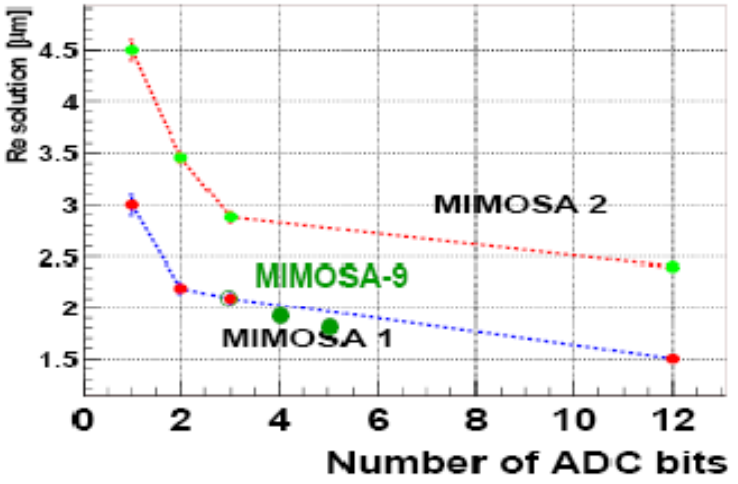


- σ_{sp} dependence on ADC granularity
  - minimise number of ADC bits
    - minimise dimensions, $t_{r.o.}$, P_{diss}
  - effect simulated on real MIMOSA data

(20 μm pitch, 120 GeV/c $\pi^{\pm}$ beam, M9, T=20 °C)

- σ_{sp} < 2 μm (4 bits ADC)
- σ_{sp} ~ 1.6-1.7 μm (5 bits ADC)

  - results based on simple pixel (N~≤10 e^-)
    - rad.tol. pixel integrating CDS (N ~≤ 15 e^-) not yet evaluated



Fast read-out sensors
with // read-out and digital output

Discri. , ADC, ∅ suppression

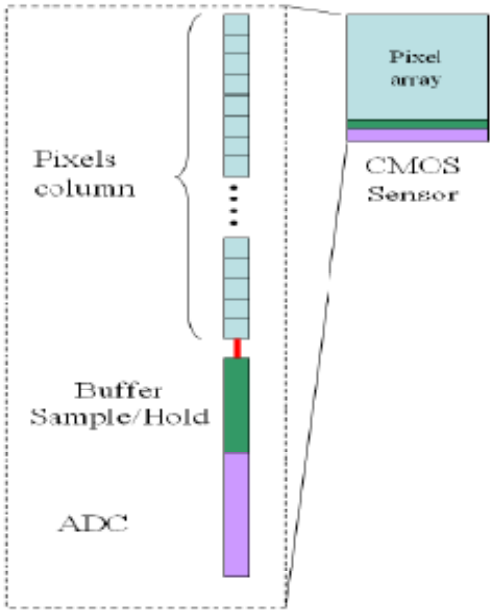
Fast read-out architecture

- Parallel development of 3 components
  - column // arrays with CDS/pixel and discriminated output
  - 4-5 bit ADCs intended to replace discriminators
  - ∅ µcircuits & output memories

- 2 stages approach
  - develop sensors for mid-term applications (2009)

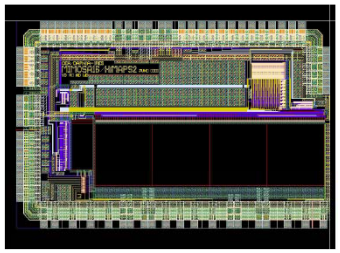
    (less severe requirements)
    - EUDET: 1x2 cm^2, tr.o. ~100 µs, discri. binary charge encoding (no ADC)
    - STAR: 2x2 cm^2, tr.o. ~200 µs, discri. binary charge encoding (no ADC)

    ⇨ will be operated in real experimental conditions by 2009/2011
  - develop ILC sensors (mainly for inner layer) extrapolated from EUDET & STAR
    - increase row rad-out frequency by ~50%
    - replace discriminators by ADCs



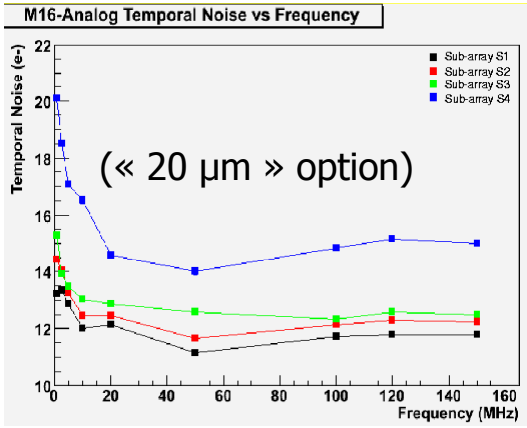
MIMOSA-16

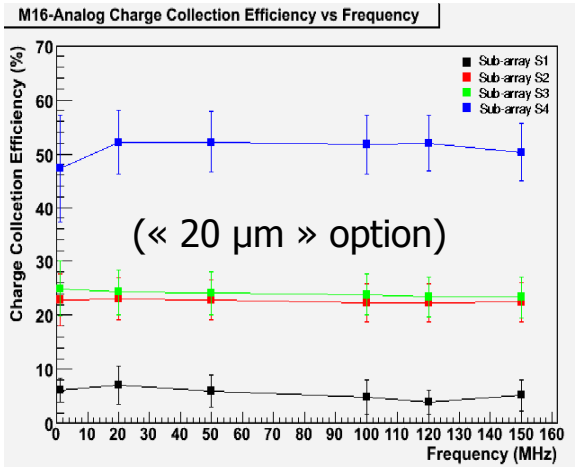
- Features: M8 (TSMC 0.25 µm) translation in AMS-OPTO 0.35 µm techno.
  - ~11 (« 14 ») AND 15 µm (« 20 ») epi layer instead of < 7 µm
  - 32 // columns of 128 pixels (pitch 25 µm), 24 ended with Discriminator
  - on pixel CDS; 4 sub arrays (various diode size, rad. hard pixels, enhanced in pixel amplification against noise of read-out chain)



- Preliminary tests of analog part (”20 µm” epi.) performed in Saclay:
  - sensors illuminated with ^{55}Fe source and r.o. frequency varied up to ≥~ 150 MHz
  - measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs $F_{r.o.}$
  - tests of analog part (« 14 » epitaxy) started in Saclay first results (CCE)
    - ➢ noise performance satisfactory (like MIMOSA-8 and -15)
    - ➢ CCE: very poor for S1 (1.7x1.7 µm^2) & poor for S2/S3 (2.4x2.4 µm^2)

  - already observed with MIMOSA-15 but more pronounced for ”20 µm” option
  - suspected origin: diffusion of P-well, reducing the N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 µm^2 diode)





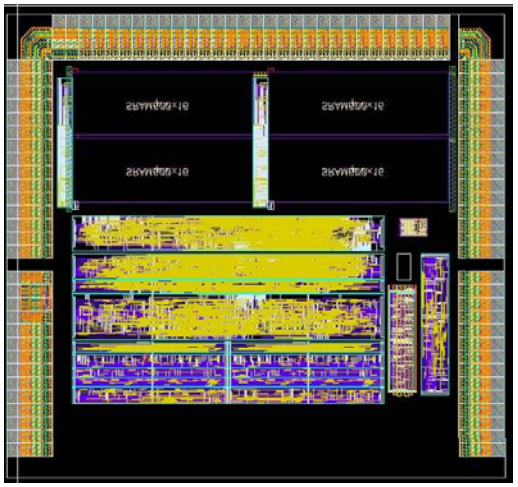
- Next steps :
  - tests of analog part (« 14 »µm epitaxy) started in Saclay
  - digital part: June 2007 at IPHC
  - beam tests in September 2007 at CERN (T4 – H6)

Zero suppression: Block diagram and 1st proto.

- Chip read-out architecture including digitisation and zero suppression
  - pixel array: 1024 x 1024 pixels read-out row by row.
    - 16 groups of rows.
    - ADC at the bottom of each column
  - zero suppression algorithm
    - find M Hits for each row
    - find N Hits for each group

    } N and M determined by occupancy rate
    - memory which stores M hits and serial transmission

- SUZE-01 : small fully digital prototype in AMS 0.35 µm



  - 2 step, line by line, logic (adapted to EUDET and STAR):
    - step-1 (inside blocks of 64 columns) : identify up to 6 series of 4 neighbour pixels per line delivering signal > discriminator threshold
    - step-2 : read-out outcome of step-1 in all blocks and keep up to 9 series of 4 neighbour pixels
  - 4 output memories (512x16 bits) taken from AMS I.P. library
  - surface 3.6 x 3.6 mm^2
  - status :
    - design under way
    - submission scheduled for end of June 2007
    - back from foundry end of September 2007
    - tests completed by end of year

ADC Developments

- Several different ADC architecture under development @IN2P3 and DAPNIA
  - LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5- and 4-bit ADC for a column pair
  - LPCC (Clermont): flash 4+1.5-bit ADC for a column pair
  - DAPNIA (Saclay): Ampli + SAR (4- and) 5-bit ADC
  - IPHC (Strasbourg): SAR 4-bit and Wilkinson 4-bit ADCs

Lab	proto	Phase	bits	chan.	$F_{r.o.}$ (MHz)	dim. (µm²)	$P_{diss.}$(µW)	eff. bits	Problems
LPSC	ADC1	test	5	8	15-25	43 x 1500	1700	4	Offset & N
	ADC2	test	5	8	15-25	43 x 1500	1700		
	ADC3	fab	4	8	25	40 x 943	800		
	ADC4	design	5	8 - 64	25	40 X 1100	900		
LPCC	ADC1	test	5.5	1	5(T)-10(S)	230 x 400	20 000	2.5	$P_{diss.}$ & bits
	ADC2	fab	5.5	1	10	40 X 1100	1000		
DAPNIA	ADC1	test	5	4	4	25 x 1000	300	≥~ 2*	missing bits
	ADC2	fab	5	4	4	25 x 1000	300		
IPHC	ADC1	test	4	16	10	25 x 1385	660		
	ADC2	test	4	16	10	25 x 1540	545		

- First mature ADC (LPSC) design expected to come out before spring 2008
  - submission of 1st col. // pixel array prototype hosting integrated ADCs in spring 2008
  - integrated ∅ zero supp. in 2009

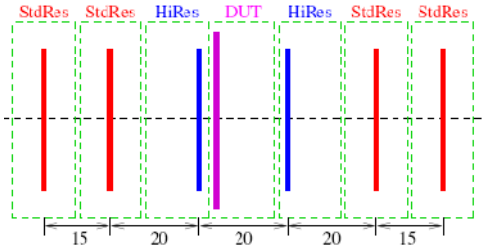
** 2 bits if LSB=1 mV, 5 bits if LSB = 20 mV

Miscellaneous

Roadmap & other developments

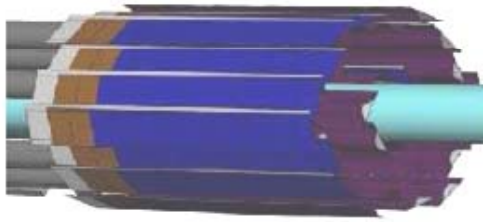
roadmap / other developments

- EUDET
  - 2 arms of 3 planes (1-2 high resolution plane)
  - provide ~1 µm resolution on 3 GeV e– beam (DESY)
  - 2 steps : 2007 (analog outputs) & 2009 (digital outputs)

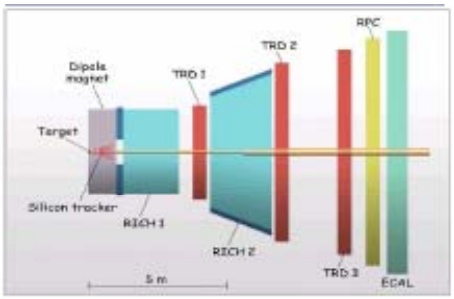


- STAR
  - 2 cylindral layers : 2000/3000 cm^2
  - 500 millions pixels (30 µm pitch)
  - resolution requirements ~≤ 8 µm
  - non ionising radiation hardness (@ room T)
  - MIMOSA-8 results : ~ 7-8 µm resolution with a 25 µm pitch

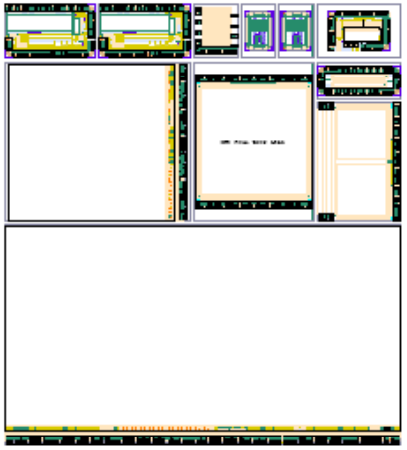
  ⇨ discri output, with pitch ≤ 20 µm
  - 2 steps : 2008 (analog outputs) & 2011 (digital outputs)



- CBM
  - 3 rectangular layers : 2000 cm^2
  - 200–300 milion pixels (20–30 µm pitch)

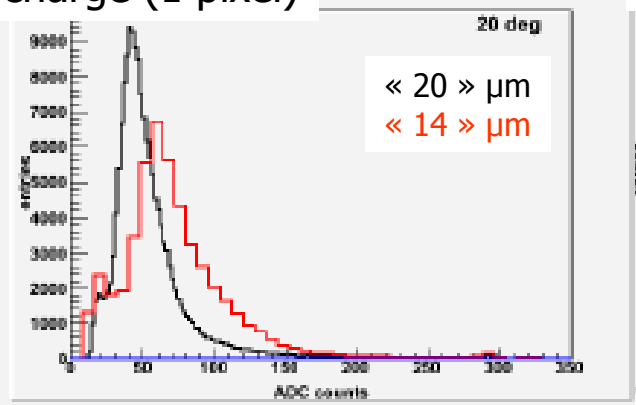


MIMOSTAR-3 (=M-20)

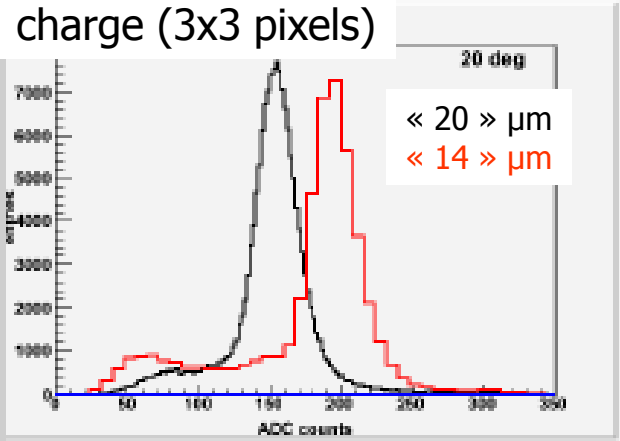


- Features
  - AMS-OPTO engineering run, fabricated in summer 2006.
  - 2+4 wafers; 2 epi layers options (« 14 » & « 20 » µm)
  - 200 k-pixels, ~2 cm^2, $t_{r.o.}$ ~ 4 ms
- Applications
  - STAR : first step (analog output)
  - EUDET: demonstrator (1kframe/s) adapted for standard resolution plane
  - ILC: discri replaced by ADC ⇨ fulfill Layers 3-4-5 requirements.

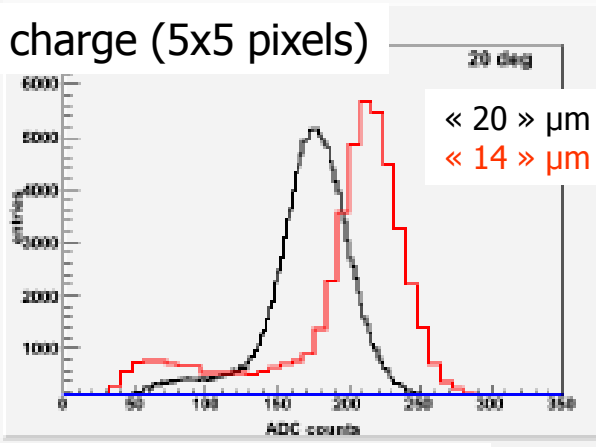
charge (1 pixel)



charge (3x3 pixels)



charge (5x5 pixels)



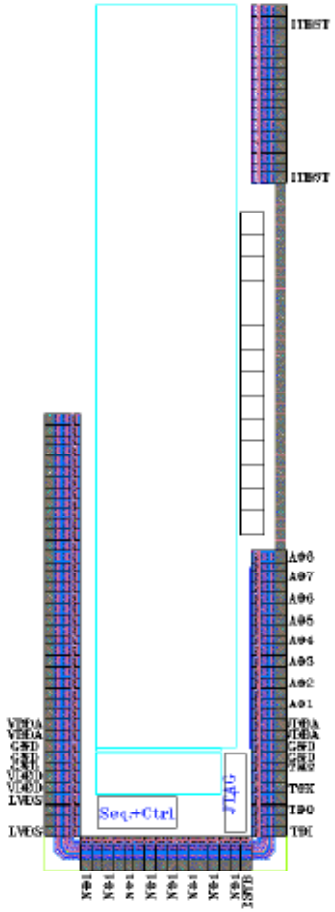
■ MIMOSA-20 ("14" & "20" μm epitaxy) illuminated with ^{55}Fe source

⟶ charge collected in seed pixel, 2x2, 3x3 and 5x5 clusters

⟶ **CCE ("14" μm) ~ 30–40 % higher than CCE ("20" μm)**

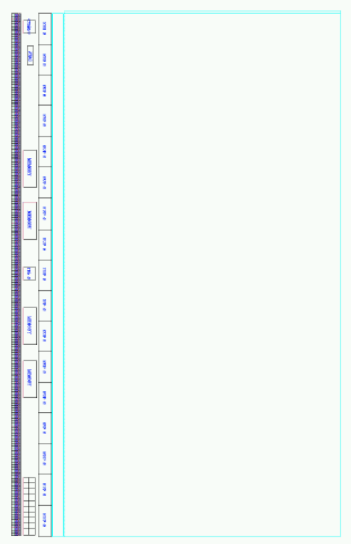
Next prototype with column // architecture : MIMOSA-22

- Extension of MIMOSA-16
  - ⇨larger surface, smaller pitch, optimised pixel, JTAG, more testability
- Pixel characteristics (still under studies)
  - pitch = 18.4 µm (compromise resolution/pixel layout)
  - diode surface ~ 10-20 µm^2 (to optimise charge coll. eff. & gain)
  - 64 columns ended with discriminator
  - 8 columns with analog output (test purposes)
  - ≥ 8 sub-matrices (≥ 4 pixels designs w/o ion. rad. tol. diode)
    - active digital area : 64 x 544-576 pixels
- Status ⇨ design underway @ IPHC and DAPNIA.
  - submission end of September 2007



Roadmap towards the Final Chip for EUDET & STAR ⇨ILC

- Spring 2008: MIMOSA-22+
  - MIMOSA-22 + ∅ (SUZE-01)
  - 1 or 2 subarrays
  - large surface: ~ 1x0.5 cm^2 (~500 pixels in column)
    - ➢ ≥~ ¼ of final number of columns (256 / 1088)



- End 2008 / early 2009: Final chip for EUDET
  - extension of MIMOSA-22+
  - 1088 col x 544/576 pixels (1x2 cm^2) ⇨engineering run
  - read-out time ~ 100 µs

- Next steps for ILC
  - incorporate ADC (with integrated discrimination) ⇨ outer layers
  - increase frequency by ~ 50 % (new ∅ and memory design)⇨ inner layers

Summary

- CMOS sensors developed for running conditions
  - ➢ with beam background >> MC simulation (sizeable occupancy uncertainty)
- General performances well established
  - eff., S/N, fake hits, resolution, rad. hardness, moderate cooling
  - AMS 0.35 µm OPTO techno assessed. ⇨Baseline for R & D
  - new generation of full scale sensors underway:
    - ➢ real experimental conditions: equip STAR, EUDET, CBM demonstrator in 2007/2008
- Fast read-out sensors progressing steadily
  - column // architecture with integrated discri. operationnal
  - ADCs close to final design
  - ∅ µcircuits: 1st generation close to fabrication
- Milestones
  - EUDET/STAR: final sensors with discri. binary charge encoding (2009 and 2010 resp.)
  - replace discris by ADCs. Increase final read-out frequency
  - find the final fabrication process (~< 0.2 µm)
- Not covered by this talk:
  - integration issues
  - thinning : (see Marco/Devis talk)
  - exploration of new fab. process (ST µ-electronics 0.25 µm) ⇨M21 under test.

back up slides

Constraints from beamstrahlung

- 1st layer (L0) : $\gtrsim$ 5 hits/cm^2/BX for 4T / 500 GeV / R_0 = 1.5 cm / no safety factor
  $\hookrightarrow \lesssim 1.8 \cdot 10^{12}$ e$^{\pm}$/cm^2/yr (safety factor of 3)
  - 2nd layer: 8 times less (direct)
  - 3rd layer: 25 times less (direct)

- Consequences on Occupancy in 1st layer (L0): $\lesssim$ 0.9 % hit occupancy in 50 μs (r.o. time of TESLA TDR)
  $\hookrightarrow$ signal spread on $\lesssim$ 4.5–9 % pixels (cluster multiplicity $\sim$ 5-10)

  $\Rightarrow$ 1) aim for shorter read-out time in L0 than in TDR $\rightarrowtail$ typically $\lesssim$ 25 μs
  (compromise with power dissipation, multiple scattering, ...)

  2) aim for shorter read-out time in L1 than in TDR $\rightarrowtail$ typically $\sim$ 50 μs (vs 250 μs)
  and presumably smaller radius (e.g. $\sim$ 20 – 22 mm)
  (use tracks extrapolated from L1-4 down to L0)

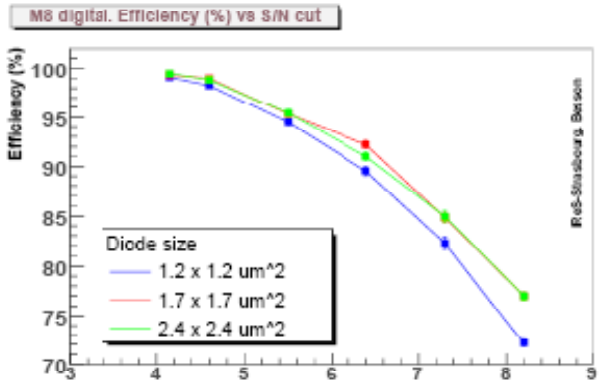
  3) aim for relaxed read-out time in L2, L3, L4: $\sim$ 100 – 200 μs (vs 250 μs)
  $\hookrightarrow$ depends on backscattered e$^{\pm}$ rate

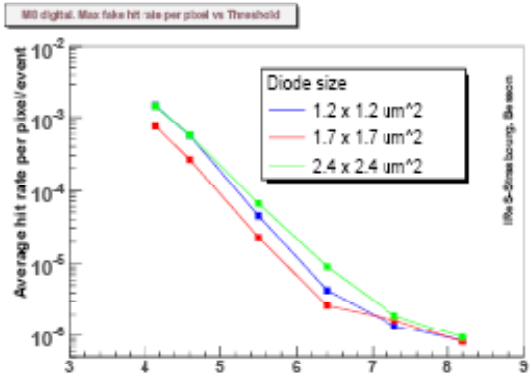
- Consequences on Radiation Tolerance in L0 :
  - dose integrated over 3 years: $\lesssim 5.4 \cdot 10^{12}$ e/cm^2 $\longrightarrow \lesssim 2 \cdot 10^{11}$ n$_{eq}$/cm^2 (NIEL $\sim$ 1/30)
    - neutron dose integrated over 3 years much smaller : $\lesssim 3 \cdot 10^{10}$ n$_{eq}$/cm^2 (safety factor of 10)

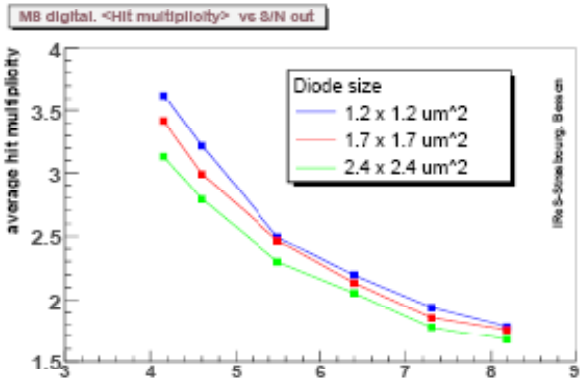
MIMOSA-8

- MIMOSA-8: TSMC 0.25 μm digital fab. process ($< 7\ \mu m$ epitaxy)
  - 32 // columns of 128 pixels (pitch: 25 μm)
  - read-out time $\sim$ 50 μs (resp. 20 μs) with (resp. without) DAQ
  - on-pixel CDS
  - discriminator (and DS) integrated at end of each of 24 columns

- Detection performance with 5 GeV/c e^- beam (DESY):







▷▷ Excellent m.i.p. detection performances despite modest thickness of epitaxial layer

✳ det. eff. $\sim$ 99.3 % for fake rate of $\sim$ 0.1 % ✳ discri. cluster mult. $\sim$ 3–4 ✳ $P_{diss} \lesssim 500\ \mu W$ / col.

▷▷ Architecture validated for next steps: techno. with thick epitaxy, rad. tol. pixel at T_{room}, ADC, Ø, etc.

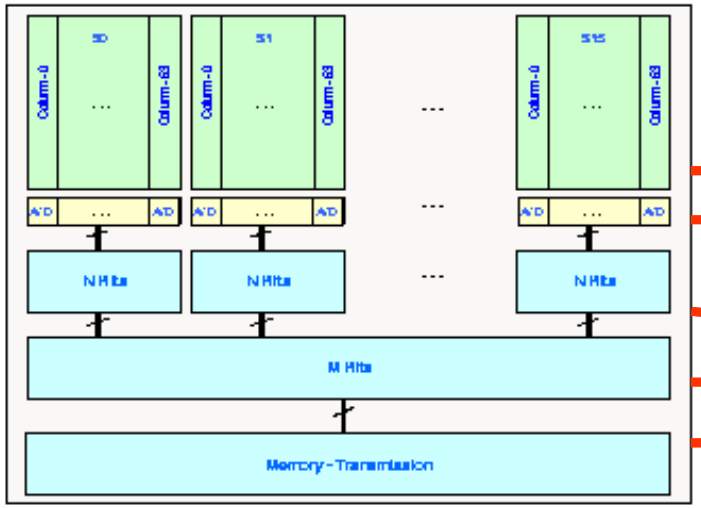
APPENDIX A: Summary of fabricated MIMOSA sensors mentionned in the report

MIMOSA-8	fabrication	2003 - TSMC-0.25 techno. - epitaxy thickness < 7 μm
	geometry	25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels
	features	column parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-9	fabrication	2003 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm (also with "high-res" substrate without epitaxy)
	geometry	20, 30 & 40 μm pitch - various pixel architectures
	features	technology exploration - analog output - serial read-out
MIMOSA-11	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
	geometry	20 & 30 μm pitch - 106x106 pixels - 4 sub-arrays
	features	analog output - serial read-out
MIMOSA-14	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
	geometry	30 μm pitch - 2 groups of 64x128 pixels
	features	STAR prototype - ionising rad. tol. pixels - analog output - serial read-out
MIMOSA-15	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
	geometry	20 & 30 μm pitch - 4 sub-arrays with various pixels
	features	non-ionising rad.tol. pixels - analog output - serial read-out
MIMOSA-16	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels
	features	column parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\gtrsim$ 6 MHz
MIMOSA-17	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	30 μm pitch - 4 groups of 64x256 pixels
	features	EUDET demonstrator - 4 analog outputs - serial read-out inside each group
MIMOSA-18	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	10 μm pitch - 512x512 pixels
	features	EUDET sensor - sub-micron resolution - analog output - serial read-out inside each group
MIMOSA-20	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	30 μm pitch - ionising rad.tol.pixels - 2 groups of 320x320 pixels
	features	STAR demonstrator (final prototype) - 2 analog outputs - serial read-out inside each group
MIMOSA-21	fabrication	2006 - STM-0.25 BICMOS techno. - sensitive volume includes "high-res" substrate
	geometry	128x192 pixels with 10 μm pitch - 64x96 pixels with 20 μm pitch
	features	beta-imager - analog outputs - serial read-out

APPENDIX B: Sensors and micro-circuits to be fabricated $\leq$ 2010

MIMOSA-22	fabrication	2007 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET	geometry	18 μm pitch - 500-600 rows - 64/8 col. with digital/analog output - 6-8 sub-arrays with different pixels
and STAR.)	features	col. parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
SUZE-01	fabrication	2007 - AMS-0.35 OPTO techno. - no epitaxy
(for EUDET & STAR.)	features	zero suppression logic & memories - specific to EUDET & STAR.
MIMOSA-22+E	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET)	geometry	18 μm pitch - 500-600 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. zero suppression - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-22+S	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for STAR.)	geometry	18 μm pitch - 1088 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. zero suppression - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-22++E	fabrication	2008/2009 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET)	geometry	18 μm pitch - 500-600 rows - 1088 col. with digital output
	features	final chip equipping telescope - col. parallel read-out with integ. zero suppression - read-out time $\sim$ 100 μs
MIMOSA-22++S	fabrication	2009 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for STAR.)	geometry	18 μm pitch - 1088 rows - 1088 col. with digital output
	features	final chip for HFT col. parallel read-out with integ. 0 supp. - read-out time $\lesssim$ 200 μs
ADC	fabrication	2007/2008 - AMS-0.35 OPTO techno. - no epitaxy
(for ILC)	features	various architectures - 4 or 5 bits - $\geq$ 8 channels - specif. for EUDET & STAR.
MIMOSA16+	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 64 col. with digital output - $\geq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. ADC
SUZE-02	fabrication	2008 - AMS-0.35 OPTO techno. - no epitaxy
(for ILC)	features	0 suppression micro-circuits & memories - specific to ILC
MIMOSA-X	fabrication	2008/2009 - various technologies with $<$ 0.2 μm feature size
ADC-X	fabrication	2008/2009 - various technologies with $<$ 0.2 μm feature size
SUZE-X	fabrication	2008/2009 - selected technology with $<$ 0.2 μm feature size
MIMOSA16++	fabrication	2009 - AMS-0.35 OPTO techno.? - epitaxy thickness $\sim$ 11 μm ?
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. ADC & zero suppression
MIMOSA16+++	fabrication	2010 - technology ?
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	final sensor - col. parallel read-out with integ. ADC & 0 suppression

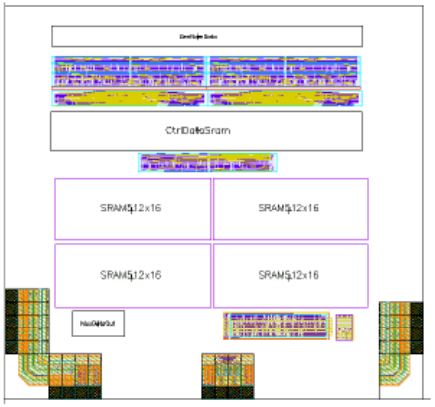
Zero suppression: Block diagram and 1st proto.



- Chip read-out architecture including digitisation and zero suppression
  - pixel array: 1024 x 1024 pixels read-out row by row.
    - 16 groups of rows.
    - ADC at the bottom of each column
  - zero suppression algorithm
    - find M Hits for each row
    - find N Hits for each group
    - memory which stores M hits and serial transmission

N and M determined by occupancy rate

- SUZE-01 : small fully digital prototype in AMS 0.35 µm
  - 2 step, line by line, logic (adapted to EUDET and STAR):
    - step-1 (inside blocks of 64 columns) : identify up to 6 series of 4 neighbour pixels per line delivering signal > discriminator threshold
    - step-2 : read-out outcome of step-1 in all blocks and keep up to 9 series of 4 neighbour pixels
  - 4 output memories (512x16 bits) taken from AMS I.P. library
  - surface 3.6 x 3.6 mm^2
  - status :
    - design under way
    - submission scheduled for end of June 2007
    - back from foundry end of September 2007
    - tests completed by end of year



Labs	No. of Chip	Phase* (D. F. T.)	No. of Bits	No. Of channels	Freq. of Readout (MHz)	Dimension (μm^2)	Power	Effective No. of Bits	Pb?
LPSC	2	T	5	8	15 - 25	43x1500 (1 ADC➔2)	1700 µW (1 ADC➔2)	4	Offset Digit noise
	1	F	4	8	25	40x943 (1 ADC➔2)	800 µW (1 ADC➔2)		
	1	D	5	+8- < 64	25	40x1100 (1 ADC➔2)	900 µW (1 ADC➔2)		

Labs	No. of Chip	Phase* (D. F. T.)	No. of Bits	No. Of channels	Freq. of Readout (MHz)	Dimension (μm^2)	Power	Effective No. of Bits	Pb?
LPCC	1	T	5.5	1	5 Test 10 Sim	230x400	20000 µW	2.5	Power x20
	1	F	5.5	1	10	40x1100	1000 µW		

Labs	No. of Chip	Phase* (D. F. T.)	No. of Bits	No. Of channels	Freq. of Readout (MHz)	Dimension (μm^2)	Power	Effective No. of Bits	Pb?
DAPNIA	1	T	5	4	4	25x1000	300 µW	2 - 5**	Missing bits
	1	F	5	4	4	25x1000	300 µW		Offset nonlinearity

Labs	No. of Chip	Phase* (D. F. T.)	No. of Bits	No. Of channels	Freq. of Readout (MHz)	Dimension (μm^2)	Power	Effective No. of Bits	Pb?
IPHC	1	T	4	16	10	25x1385	660 µW		
	1	T	4	16	10	25x1540	545 µW		

* D: Design, F: Fabrication, T: Test

** 2 bits if LSB=1 mV, 5 bits if LSB = 20 mV