Status on CMOS sensors

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on behalf of

DAPNIA/Saclay, LPSC/Grenoble, LPC/Clermont-F., DESY, Uni. Hamburg, JINR-Dubna & IPHC/Strasbourg

contributions from

IPN/Lyon, Uni. Frankfurt, GSI-Darmstadt, STAR coll.(BNL, BNL)

- ILC requirements
- Review on CMOS Performances: state of the art
- Progress on fast read-out sensors & ADC
- Roadmap for the coming years
- Summary
ILC requirements

• Beam background: 1\textsuperscript{st} layer: $\geq \sim 5$ hits/cm$^2$/BX
  - (4T, 500 GeV, $R_0 = 1.5$ cm, no safety factor)
  - $\sim 1.8 \times 10^{12}$ e$^\pm$/cm$^2$/yr (safety factor of 3)
  - occupancy:
    - keep it below $\sim$ few % (cluster multiplicity $\sim$5-10)
    - aim for a read-out time $\leq 25$ µs

• ILC vertex detector
  - 5–6 cylindrical layers: $\sim$3000 cm$^2$
  - 300-500 million pixels (20–40 µm pitch)
  - 1\textsuperscript{st} complete ladder prototype $\sim$ 2010

• Read-out speed objectives/ constraints
  - column parallel read-out $\perp$ to beam axis
  - ADC @ the end of each column
  - $\emptyset$ zero suppression $\mu$-circuits.
Review on CMOS Performances

- Detection efficiency
- Radiation hardness
- Resolution
General performances

(from H.E. beam tests @ DESY and CERN)

- Charged particle detection well established (analog output)
  - best performing technology:
    - AMS 0.35 µm OPTO
  - N~ 10 e- ⇒ S/N (MPV) 20-30
    - eff>~ 99.5 %
  - operating temperature ≥~ 40°C
  - macroscopic sensors:
    - MIMOSA-5 (1 Mpix, 3.5 cm²)
    - MIMOSA-20 (=M*3) (200 kpix, 1x2 cm²)
    - MIMOSA-17 (65 kpix, 0.8 x 0.8 cm²)

- Efficiency vs rate of fake clusters:
  - vary cut on seed pixel:
    - 6 ⇒ 12 ADC units (Noise ~1.5 ADC u.)
  - vary cut on Σ of crown charge:
    - 0,3,4,9,13,17 ADC units
  - eff ~99.9 % for fake rate ~10⁻⁵
Radiation hardness: MIMOSA-15

- **Non ionising radiation tolerance**
  - M-15 irradiated with O(1 MeV) neutrons tested with 6 GeV e- beam (DESY)
    - T = -20 °C, t_{r.o.} ~ 700 µs
    - 5.8x10^{12} n_{eq}/cm^2 values derived with standard and soft cuts

- **Ionising radiation tolerance**
  - M-15 irradiated with 10 keV X-rays up to 1 MRad (tested @ DESY)
    - pixels modified against hole accumulation (thick oxide) and leakage current increase (guard ring)
    - T = -20 °C, t_{r.o.} ~ 180 µs
    - t_{r.o.} << 1 ms crucial @ room T

- **Preliminary conclusion**
  - at least 3 years of running viable @ room T° (or close to)
  - further assessment needed
    - test 10 MeV e-
    - sensors with integrated CDS, ADC, etc.

<table>
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<tr>
<th>Fluence</th>
<th>0</th>
<th>0.47</th>
<th>2.1</th>
<th>5.8 (5/2)</th>
<th>5.8 (4/2)</th>
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<tbody>
<tr>
<td>S/N (MPV)</td>
<td>27.8 ± 0.5</td>
<td>21.8 ± 0.5</td>
<td>14.7 ± 0.3</td>
<td>&lt;&lt; 8.7 ± 2.0 &lt;&lt; 7.5 ± 2.0</td>
<td></td>
</tr>
<tr>
<td>Det. Eff. (%)</td>
<td>100.</td>
<td>99.9 ± 0.1</td>
<td>99.3 ± 0.2</td>
<td>77. ± 2</td>
<td>84. ± 2</td>
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</table>

<table>
<thead>
<tr>
<th>Integ. Dose</th>
<th>Noise</th>
<th>S/N (MPV)</th>
<th>Detection Efficiency</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>9.0 ± 1.1</td>
<td>27.8 ± 0.5</td>
<td>100 %</td>
</tr>
<tr>
<td>1 MRad</td>
<td>10.7 ± 0.9</td>
<td>19.5 ± 0.2</td>
<td>99.96 ± 0.04 %</td>
</tr>
</tbody>
</table>
Spatial Resolution vs ADC resolution

- **Single point resolution vs pitch**
  - hit position reconstructed with eta function, exploiting charge sharing between pixels
  - $\sigma_{sp} \sim 1.5 \, \mu m$ (20 $\mu m$ pitch)
  - obtained with charge encoded on 12 bits.

- **$\sigma_{sp}$ dependence on ADC granularity**
  - minimise number of ADC bits
    - minimise dimensions, $t_{r.o.}$, $P_{diss}$
  - effect simulated on real MIMOSA data
    - (20 $\mu m$ pitch, 120 GeV/c $\pi^\pm$ beam, M9, T=20 $^\circ$C)
      - $\sigma_{sp} < 2 \, \mu m$ (4 bits ADC)
      - $\sigma_{sp} \sim 1.6$-1.7 $\mu m$ (5 bits ADC)
  - results based on simple pixel ($N \sim \leq 10 \, e^-$)
    - rad.tol. pixel integrating CDS ($N \sim \leq 15 \, e^-$) not yet evaluated
Fast read-out sensors
with read-out and digital output

Discri., ADC, Ø suppression
Fast read-out architecture

- **Parallel development of 3 components**
  - column // arrays with CDS/pixel and discriminated output
  - 4-5 bit ADCs intended to replace discriminators
  - Ø µcircuits & output memories

- **2 stages approach**
  - develop sensors for mid-term applications (2009)
    (less severe requirements)
    - EUDET: 1x2 cm², tr.o. ~100 µs, discr. binary charge encoding
      (no ADC)
    - STAR: 2x2 cm², tr.o. ~200 µs, discr. binary charge encoding
      (no ADC)
    - will be operated in real experimental conditions by 2009/2011
  - develop ILC sensors (mainly for inner layer) extrapolated from EUDET & STAR
    - increase row rad-out frequency by ~50%
    - replace discriminators by ADCs
MIMOSA-16

- Features: M8 (TSMC 0.25 µm) translation in AMS-OPTO 0.35 µm techno.
  - ~11 (« 14 ») AND 15 µm (« 20 ») epi layer instead of < 7 µm
  - 32 // columns of 128 pixels (pitch 25 µm), 24 ended with Discriminator
  - on pixel CDS; 4 sub arrays (various diode size, rad. hard pixels, enhanced in pixel amplification against noise of read-out chain)

- Preliminary tests of analog part ("20 µm" epi.) performed in Saclay:
  - sensors illuminated with $^{55}$Fe source and r.o. frequency varied up to $\geq 150$ MHz
  - measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs F_r.o.
  - tests of analog part (« 14 » epitaxy) started in Saclay first results (CCE)
    - noise performance satisfactory (like MIMOSA-8 and -15)
    - CCE: very poor for S1 (1.7x1.7 µm$^2$) & poor for S2/S3 (2.4x2.4 µm$^2$)
      - already observed with MIMOSA-15 but more pronounced for "20 µm" option
      - suspected origin: diffusion of P-well, reducing the N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 µm$^2$ diode)

- Next steps:
  - tests of analog part (« 14 »µm epitaxy) started in Saclay
  - digital part: June 2007 at IPHC
  - beam tests in September 2007 at CERN (T4 – H6)
Zero suppression: Block diagram and 1\textsuperscript{st} proto.

- Chip read-out architecture including digitisation and zero suppression
  - pixel array: 1024 x 1024 pixels read-out row by row.
    - 16 groups of rows.
    - ADC at the bottom of each column
  - zero suppression algorithm
    - find M Hits for each row
    - find N Hits for each group
    - memory which stores M hits and serial transmission

- SUZE-01: small fully digital prototype in AMS 0.35 µm
  - 2 step, line by line, logic (adapted to EUDET and STAR):
    - step-1 (inside blocks of 64 columns): identify up to 6 series of 4 neighbour pixels per line delivering signal > discriminator threshold
    - step-2: read-out outcome of step-1 in all blocks and keep up to 9 series of 4 neighbour pixels
  - 4 output memories (512x16 bits) taken from AMS I.P. library
  - surface: 3.6 x 3.6 mm\(^2\)
  - status:
    - design under way
    - submission scheduled for end of June 2007
    - back from foundry end of September 2007
    - tests completed by end of year
ADC Developments

- Several different ADC architecture under development @IN2P3 and DAPNIA
  - LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5- and 4-bit ADC for a column pair
  - LPCC (Clermont): flash 4+1.5-bit ADC for a column pair
  - DAPNIA (Saclay): Ampli + SAR (4- and) 5-bit ADC
  - IPHC (Strasbourg): SAR 4-bit and Wilkinson 4-bit ADCs

<table>
<thead>
<tr>
<th>Lab</th>
<th>proto</th>
<th>Phase</th>
<th>bits</th>
<th>chan.</th>
<th>F_r.o. (MHz)</th>
<th>dim. (µm²)</th>
<th>P_diss.(µW)</th>
<th>eff. bits</th>
<th>Problems</th>
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<td>LPSC</td>
<td>ADC1</td>
<td>test</td>
<td>5</td>
<td>8</td>
<td>15-25</td>
<td>43 x 1500</td>
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<td>5</td>
<td>8</td>
<td>15-25</td>
<td>43 x 1500</td>
<td>1700</td>
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<tr>
<td></td>
<td>ADC3</td>
<td>fab</td>
<td>4</td>
<td>8</td>
<td>25</td>
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<td>800</td>
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<td>ADC4</td>
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<td>8 - 64</td>
<td>25</td>
<td>40 X 1100</td>
<td>900</td>
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<td>test</td>
<td>5.5</td>
<td>1</td>
<td>5(T)-10(S)</td>
<td>230 x 400</td>
<td>20 000</td>
<td>2.5</td>
<td>P_diss. &amp; bits</td>
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<tr>
<td></td>
<td>ADC2</td>
<td>fab</td>
<td>5.5</td>
<td>1</td>
<td>10</td>
<td>40 X 1100</td>
<td>1000</td>
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<td>test</td>
<td>5</td>
<td>4</td>
<td>4</td>
<td>25 x 1000</td>
<td>300</td>
<td>≥~ 2*</td>
<td>missing bits</td>
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<tr>
<td></td>
<td>ADC2</td>
<td>fab</td>
<td>5</td>
<td>4</td>
<td>4</td>
<td>25 x 1000</td>
<td>300</td>
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<tr>
<td>IPHC</td>
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<td>10</td>
<td>25 x 1385</td>
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<tr>
<td></td>
<td>ADC2</td>
<td>test</td>
<td>4</td>
<td>16</td>
<td>10</td>
<td>25 x 1540</td>
<td>545</td>
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</table>

- First mature ADC (LPSC) design expected to come out before spring 2008
  ➢ submission of 1st col. // pixel array prototype hosting integrated ADCs in spring 2008
  ➢ integrated ⊘ zero supp. in 2009

** 2 bits if LSB=1 mV, 5 bits if LSB = 20 mV
Miscellaneous

Roadmap & other developments
roadmap / other developments

- **EUDET**
  - 2 arms of 3 planes (1-2 high resolution plane)
  - provide \(\sim 1\ \mu m\) resolution on 3 GeV e\(^-\) beam (DESY)
  - 2 steps: 2007 (analog outputs) & 2009 (digital outputs)

- **STAR**
  - 2 cylindrical layers: 2000/3000 cm\(^2\)
  - 500 millions pixels (30 \(\mu m\) pitch)
  - resolution requirements \(\sim \leq 8\ \mu m\)
  - non ionising radiation hardness (@ room T)
  - MIMOSA-8 results: \(\sim 7-8\ \mu m\) resolution with a 25 \(\mu m\) pitch
  - discr output, with pitch \(\leq 20\ \mu m\)
  - 2 steps: 2008 (analog outputs) & 2011 (digital outputs)

- **CBM**
  - 3 rectangular layers: 2000 cm\(^2\)
  - 200–300 milion pixels (20–30 \(\mu m\) pitch)
MIMOSTAR-3 (=M-20)

- **Features**
  - AMS-OPTO engineering run, fabricated in summer 2006.
  - 2+4 wafers; 2 epi layers options («14» & «20» µm)
  - 200 k-pixels, ~2 cm², t_{r.o.} ~ 4 ms

- **Applications**
  - STAR: first step (analog output)
  - EUDET: demonstrator (1kframe/s) adapted for standard resolution plane
  - ILC: discri replaced by ADC ⇒ fulfill Layers 3-4-5 requirements.

Charge (1 pixel) | Charge (3x3 pixels) | Charge (5x5 pixels)

MIMOSA-20 (”14” & ”20” µm epitaxy) illuminated with ^{55}Fe source

→ charge collected in seed pixel, 2x2, 3x3 and 5x5 clusters

→ CCE (”14” µm) ~ 30–40 % higher than CCE (”20” µm)
Next prototype with column // architecture : MIMOSA-22

- Extension of MIMOSA-16
  -更大表面，更小间隔，优化像素，JTAG，更多可测试性

- Pixel characteristics (still under studies)
  - pitch = 18.4 µm (compromise resolution/pixel layout)
  - diode surface ~ 10-20 µm² (to optimise charge collect. eff. & gain)
  - 64 columns ended with discriminator
  - 8 columns with analog output (test purposes)
  - ≥ 8 sub-matrices (≥ 4 pixels designs w/o ion. rad. tol. diode)
    - active digital area : 64 x 544-576 pixels

- Status ⇒ design underway @ IPHC and DAPNIA.
  - submission end of September 2007
Roadmap towards the Final Chip for EUDET & STAR ⇒ ILC

• Spring 2008: MIMOSA-22+
  – MIMOSA-22 + ∅ (SUZE-01)
  – 1 or 2 subarrays
  – large surface: ~ 1x0.5 cm² (~500 pixels in column)
    ➢ ≥~ ¼ of final number of columns (256 / 1088)

• End 2008 / early 2009: Final chip for EUDET
  – extension of MIMOSA-22+
  – 1088 col x 544/576 pixels (1x2 cm²) ⇒ engineering run
  – read-out time ~ 100 µs

• Next steps for ILC
  – incorporate ADC (with integrated discrimination) ⇒ outer layers
  – increase frequency by ~ 50 % (new ∅ and memory design) ⇒ inner layers
Summary

• **CMOS sensors developed for running conditions**
  - with beam background >> MC simulation (sizeable occupancy uncertainty)

• **General performances well established**
  - eff., S/N, fake hits, resolution, rad. hardness, moderate cooling
  - AMS 0.35 µm OPTO techno assessed. ⇒Baseline for R & D
  - new generation of full scale sensors underway:
    - real experimental conditions: equip STAR, EUDET, CBM demonstrator in 2007/2008

• **Fast read-out sensors progressing steadily**
  - column // architecture with integrated discri. operationnal
  - ADCs close to final design
  - Ø µcircuits: 1st generation close to fabrication

• **Milestones**
  - EUDET/STAR: final sensors with discri. binary charge encoding (2009 and 2010 resp.)
  - replace discris by ADCs. Increase final read-out frequency
  - find the final fabrication process (〜< 0.2 µm)

• **Not covered by this talk:**
  - integration issues
  - thinning : (see Marco/Devis talk)
  - exploration of new fab. process (ST µ-electronics 0.25 µm) ⇒M21 under test.
back up slides
Constraints from beamstrahlung

1st layer (L0): \( \gtrsim 5 \text{ hits/cm}^2/\text{BX} \) for 4T / 500 GeV / \( R_0 = 1.5 \text{ cm} \) / no safety factor
\[ \Rightarrow \lesssim 1.8 \times 10^{12} \text{ e}/\text{cm}^2/\text{yr} \] (safety factor of 3)

- 2nd layer: 8 times less (direct)
- 3rd layer: 25 times less (direct)

Consequences on Occupancy in 1st layer (L0):
\[ \lesssim 0.9 \% \text{ hit occupancy in } 50 \mu s \text{ (r.o. time of TESLA TDR)} \]
\[ \Rightarrow \text{ signal spread on } \lesssim 4.5-9 \% \text{ pixels (cluster multiplicity } \sim 5-10) \]

1) aim for shorter read-out time in L0 than in TDR \( \Rightarrow \) typically \( \lesssim 25 \mu s \)
   (compromise with power dissipation, multiple scattering, ...)
2) aim for shorter read-out time in L1 than in TDR \( \Rightarrow \) typically \( \sim 50 \mu s \) (vs 250 \( \mu s \))
   and presumably smaller radius (e.g. \( \sim 20 - 22 \text{ mm} \))
   (use tracks extrapolated from L1-4 down to L0)
3) aim for relaxed read-out time in L2, L3, L4: \( \sim 100 - 200 \mu s \) (vs 250 \( \mu s \))
   \( \Rightarrow \text{ depends on backscattered } e^\pm \text{ rate} \)

Consequences on Radiation Tolerance in L0:

- dose integrated over 3 years: \( \lesssim 5.4 \times 10^{12} \text{ e}/\text{cm}^2 \)
  \[ \Rightarrow \lesssim 2 \times 10^{11} \text{ n}_{eq}/\text{cm}^2 \] (NIEL \( \sim 1/30 \))

- neutron dose integrated over 3 years much smaller: \( \lesssim 3 \times 10^{10} \text{ n}_{eq}/\text{cm}^2 \) (safety factor of 10)
MIMOSA-8: TSMC 0.25 \( \mu m \) digital fab. process (< 7 \( \mu m \) epitaxy)
- 32 \parallel \) columns of 128 pixels (pitch: 25 \( \mu m \))
- read-out time \( \sim 50 \mu s \) (resp. 20 \( \mu s \)) with (resp. without) DAQ
- on-pixel CD8
- discriminator (and DS) integrated at end of each of 24 columns

Detection performance with 5 GeV/c \( e^- \) beam (DESY):

- Excellent m.i.p. detection performances despite modest thickness of epitaxial layer
  - det. eff. \( \sim 99.3 \% \) for fake rate of \( \sim 0.1 \% \)
  - discr. cluster mult. \( \sim 3-4 \)
  - \( P_{diss} \leq 500 \mu W / col. \)
- Architecture validated for next steps: techno. with thick epitaxv. rad. tol. pixel at \( T_{room} \), ADC. \( \Theta \), etc.
## APPENDIX A: Summary of fabricated MIMOSA sensors mentioned in the report

<table>
<thead>
<tr>
<th>MIMOSA-8</th>
<th>fabrication 2003 - TSMC-0.25 techno. - epitaxy thickness &lt; 7 μm</th>
<th>geometry 25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels</th>
<th>features column parallel read-out - clock frequency ≥ 100 MHz - row read-out frequency ~ 6 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIMOSA-9</td>
<td>fabrication 2003 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 μm (also with &quot;high-res&quot; substrate without epitaxy)</td>
<td>geometry 20, 30 &amp; 40 μm pitch - various pixel architectures</td>
<td>features technology exploration - analog output - serial read-out</td>
</tr>
<tr>
<td>MIMOSA-11</td>
<td>fabrication 2005 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 μm</td>
<td>geometry 20 &amp; 30 μm pitch - 106x106 pixels - 4 sub-arrays</td>
<td>features analog output - serial read-out</td>
</tr>
<tr>
<td>MIMOSA-14</td>
<td>fabrication 2005 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 μm</td>
<td>geometry 30 μm pitch - 2 groups of 64x128 pixels</td>
<td>features STAR prototype - ionising red. tol. pixels - analog output - serial read-out</td>
</tr>
<tr>
<td>MIMOSA-15</td>
<td>fabrication 2005 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 μm</td>
<td>geometry 20 &amp; 30 μm pitch - 4 sub-arrays with various pixels</td>
<td>features non-ionising red. tol. pixels - analog output - serial read-out</td>
</tr>
<tr>
<td>MIMOSA-16</td>
<td>fabrication 2006/7 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 &amp; 15 μm</td>
<td>geometry 25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels</td>
<td>features column parallel read-out - clock frequency ≥ 100 MHz - row read-out frequency ≥ 6 MHz</td>
</tr>
<tr>
<td>MIMOSA-17</td>
<td>fabrication 2006/7 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 &amp; 15 μm</td>
<td>geometry 30 μm pitch - 4 groups of 64x256 pixels</td>
<td>features BUTET demonstration - 4 analog outputs - serial read-out inside each group</td>
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<tr>
<td>MIMOSA-18</td>
<td>fabrication 2006/7 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 &amp; 15 μm</td>
<td>geometry 10 μm pitch - 512x512 pixels</td>
<td>features BUTET sensor - sub-micron resolution - analog output - serial read-out inside each group</td>
</tr>
<tr>
<td>MIMOSA-20</td>
<td>fabrication 2006/7 - AMS-0.35 opto techno. - epitaxy thickness ~ 11 &amp; 15 μm</td>
<td>geometry 30 μm pitch - ionising red.tol. pixels - 2 groups of 320x320 pixels</td>
<td>features STAR demonstrator (final prototype) - 2 analog outputs - serial read-out inside each group</td>
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<tr>
<td>MIMOSA-21</td>
<td>fabrication 2008 - STM-0.25 eXtreme techno. - sensitive volume includes &quot;high-res&quot; substrate</td>
<td>geometry 128x192 pixels with 10 μm pixels - 64x96 pixels with 20 μm pixels</td>
<td>features beta-imager - analog outputs - serial read-out</td>
</tr>
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# APPENDIX B: Sensors and micro-circuits to be fabricated ≤ 2010

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Fabrication Year</th>
<th>Technology</th>
<th>Epitaxy Thickness</th>
<th>Features</th>
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<td>MIMOSA-22</td>
<td>2007</td>
<td>AMS-0.35 ORO technology</td>
<td>~11 μm</td>
<td>- 18 μm pitch - 500-800 rows - 64/8 col. with digital/analog output - 6-8 sub-arrays with different pixels</td>
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<tr>
<td>(for EUDET)</td>
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</tr>
<tr>
<td>and STAR)</td>
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<tr>
<td>SUZE-01</td>
<td>2007</td>
<td>AMS-0.35 ORO technology</td>
<td>- no epitaxy</td>
<td>- zero suppression logic &amp; memories - specific to EUDET &amp; STAR</td>
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<td>(for EUDET &amp; STAR)</td>
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<tr>
<td>MIMOSA-22+S</td>
<td>2008</td>
<td>AMS-0.35 ORO technology</td>
<td>~11 μm</td>
<td>- 18 μm pitch - 500-800 rows - &gt; 258 col. with digital output - ≤ 2 sub-arrays with different pixels</td>
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<td>(for STAR)</td>
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<td>- 18 μm pitch - 500-800 rows - &gt; 258 col. with digital output - ≤ 2 sub-arrays with different pixels</td>
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<td>(for EUDET)</td>
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<tr>
<td>MIMOSA-22+S+S</td>
<td>2009</td>
<td>AMS-0.35 ORO technology</td>
<td>~11 μm</td>
<td>- 18 μm pitch - 1088 rows - &gt; 258 col. with digital output - ≤ 2 sub-arrays with different pixels</td>
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<td>(for STAR)</td>
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<td>- no epitaxy</td>
<td>- various architectures - 4 or 5 bits - ≤ 8 channels - specific for EUDET &amp; STAR</td>
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<td>~11 μm</td>
<td>- 20-22 μm pitch - 258-320 rows - ≥ 64 col. with digital output - ≥ 2 sub-arrays with different pixels</td>
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Zero suppression: Block diagram and 1st proto.

- Chip read-out architecture including digitisation and zero suppression
  - pixel array: 1024 x 1024 pixels read-out row by row.
    - 16 groups of rows.
    - ADC at the bottom of each column
  - zero suppression algorithm
    - find M Hits for each row
    - find N Hits for each group
    - memory which stores M hits and serial transmission
    \[ N \text{ and } M \text{ determined by occupancy rate} \]

- SUZE-01: small fully digital prototype in AMS 0.35 µm
  - 2 step, line by line, logic (adapted to EUDET and STAR):
    - step-1 (inside blocks of 64 columns): identify up to 6 series of 4 neighbour pixels per line delivering signal > discriminator threshold
    - step-2: read-out outcome of step-1 in all blocks and keep up to 9 series of 4 neighbour pixels
  - 4 output memories (512x16 bits) taken from AMS I.P. library
  - surface 3.6 x 3.6 mm²
  - status:
    - design under way
    - submission scheduled for end of June 2007
    - back from foundry end of September 2007
    - tests completed by end of year
<table>
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<th>Labs</th>
<th>No. of Chip</th>
<th>Phase*</th>
<th>No. of Bits</th>
<th>No. Of channels</th>
<th>Freq. of Readout (MHz)</th>
<th>Dimension (µm²)</th>
<th>Power</th>
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* D: Design, F: Fabrication, T: Test
** 2 bits if LSB=1 mV, 5 bits if LSB = 20 mV