Optimization of amplifiers for Monolithic Active Pixel Sensors

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Abstract

High precision particle tracking and imaging applications require position sensitive detectors with high granularity, good radiation tolerance, low material budget, fast read-out and low power dissipation. Monolithic Active Pixel Sensors (MAPS) [1] fabricated in a standard microelectronic technology provide an attractive solution for these demanding applications. The signal-to-noise ratio of MAPS can be increased by using in-pixel amplifiers. The compromise between speed, noise, gain and power consumption has to be achieved in the design of the amplifier. The charge collection efficiency and total capacitance at the amplifier input is influenced by the size of charge collecting diode. Therefore, in order to achieve better MAPS performances, both the geometry of the charge collecting diode and the amplifier design have to be considered in the optimization process. In this work different amplifier designs and geometries of the charge collecting diode are proposed. The characterization measurements of the amplifiers fabricated in 0.35 µm technology will be presented. The electronic properties of the amplifiers calculated with Spectre circuit simulator [2] and the charge collection efficiency simulated with ISE-TCAD package [3] will be compared with the measurements. The advantages and drawbacks of the implemented designs will be discussed.

I. Introduction

Semiconductor position sensitive detectors are used in high precision particles tracking and imaging applications.

Moving electron-hole pairs created in a pixelized semiconductor volume induce a current at the electrodes. The signal current is amplified, processed and read out by the corresponding electronics. The peculiarity of MAPS is that the front-end electronics is implemented in a standard CMOS technology substrate, which is used as sensitive volume, contrary to all other types like CCD, hybrid pixel detectors, 3D electronics detectors (Figure 1).

The advantage of MAPS is their low cost due to usage of standard CMOS technology and the possibility to implement amplification and complex data processing in the same chip. Certainly, this implies restrictions for the architecture of electronics in MAPS: the front-end amplifier which is placed directly in the pixel sensitive volume can use only one type of MOS transistors, unless expensive technologies with isolated transistors have been utilized.

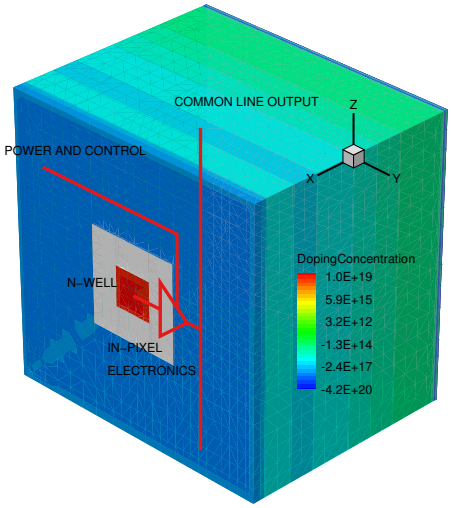

Figure 1: Basic pixel cell: nwell in p-type substrate, the readout electronics is placed in the substrate between the nwells.

In addition to this, usage of low resistivity (10-200 $\Omega \cdot$ cm) substrate in the standard CMOS technology makes it possible to deplete only a very small fraction of the detector sensitive volume, and the electron-hole pairs transport is dominated by thermal diffusion.

II. Objectives and possible solutions

MAPS based on CMOS technology being developed in Strasbourg [4], have become increasingly competitive candidates for vertexing detectors for the International Linear Collider and STAR experiment at the Relativistic Heavy Ion Collider. The spatial resolution and tracking performances of detectors equipped with MAPS are improved with increase of signal-to-noise ratio of in-pixel amplifier. Therefore, the objective is to develop in-pixel amplifier which achieves:

- maximum of signal-to-noise ratio for a given pixel pitch size and nwell charge collecting diode size
- minimum of power consumption
- small pixel-to-pixel performance variation due to CMOS process variation

The noise contribution to the signal after the amplifier can be significant, thus in order to maximize signal-to-noise ratio one need to obtain higher amplifier gain. Standard common source schematics (Figure 2, left) can

be utilized, however they have not sufficient voltage gain (< 5), when only nmos transistors has to be used in design:

$$Gain = V_{out}/V_{in} = \frac{g_{m1}}{(g_{m2} + g_{mb2} + g_{ds1} + g_{ds2})}$$

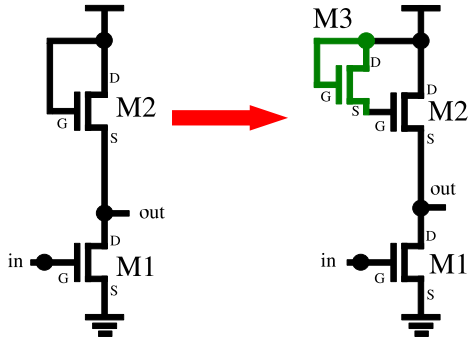

Figure 2: Standard (left) and improved (right) amplifier schematics.

Special biasing with transistor M3 (see Figure 2) for the load transistor (M2) has been introduced [5], and the gain of the improved schematic increases, due to the cancellation of g_{m2} for frequencies large than g_{m3}/C_{gs2}:

$$Gain = V_{out}/V_{in} = \frac{g_{m1}}{(g_{mb2} + g_{ds1} + g_{ds2})}$$

The AC gain of the improved amplifier increases by about a factor of two, but the DC operation point and DC gain are almost not changed, which makes the circuit more resistant to CMOS process variation. In addition to this, negative feedback can be used to stabilize the operation point of the amplifier. As a higher gain can be achieved with the same g_{m1}, one can slightly decrease g_{m1}, which can be performed by decreasing the drain current and the power consumption will decrease.

III. In-pixel amplifiers

The improved amplifier is equipped with the negative feedback. The feedback is a low pass filter with very large time constant ($C1/g_{m4}$), it also provides biasing via high resistive D2 for the charge collecting diode D1, and does not decrease the AC gain. As the reverse leakage current of diode D1 is very small, typically it is a few fA, the forward biased diode D1 has large small-signal resistance and the induced signal current is converted to a voltage at the input parasitic capacitance. With this type of feedback one can construct two circuits: one based on improved common source (Figure 3, left) and one on improved cascode (Figure 3, right).

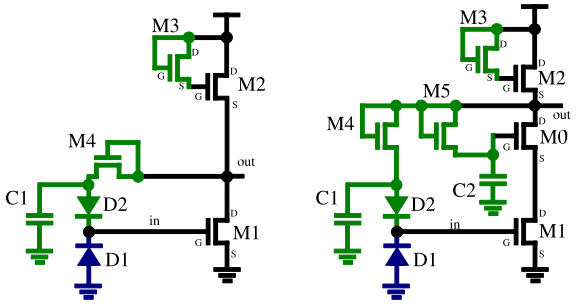

Figure 3: Common source and cascode schematics with feedback, the improved load use to increase the gain.

The low pass filter and diodes capacitances discharge time are very large, so there will be unwanted memorization of some fraction of signal, however reduced by the correlated double sampling (CDS).

A better approach is to use time variant feedback (Figure 4), where the DC operational point is set by a short pulse (set). The advantage of this schematic its simplicity and even higher gain, the disadvantage is large crosstalk to the sensing diode (D1) from the switch transistor (M3).

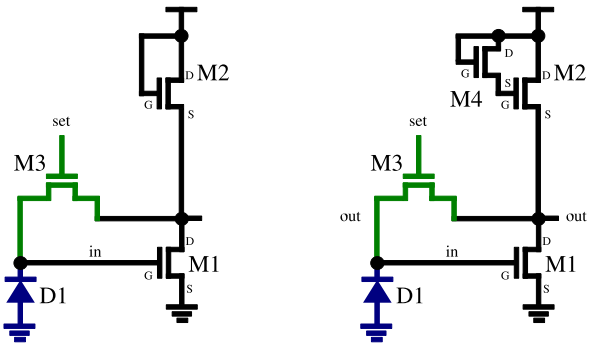

Figure 4: Amplifiers with time variant feedback. Left: standard schematic, right: improved schematic.

One can reduce the crosstalk by lowering down the controlling voltage pulse, or by increasing the diode size and hence its capacitance.

Each pixel has a CDS circuit based on the clamping technique: i.e. the first sample is the amplifier output voltage stored at the clamping capacitance, the second sample is subtracted from the stored voltage. The pixel signal after CDS is buffered by the source follower and connected via switch to common column readout line.

IV. Layouts implemented in the test chip

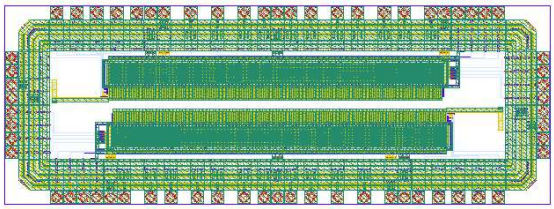

Figure 5: The layout of the test chip.

The test chip is fabricated in 0.35 µm technology (Figure 5), the pixel pitch size is 25 µm, the epitaxial layer thickness is 20 µm. In order to achieve better MAPS performances, both the geometry of the charge collecting diode and the amplifier design are considered in the optimization process. Two different nwell diode shapes were tested: square and L-shaped(Figure 6).

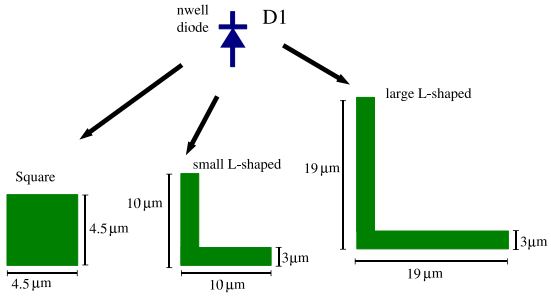

Figure 6: The layouts of tested diodes.

The designed and fabricated layouts are summarized in Table 1.

Design name	schematic	feedback	nwell diode	size of the side of nwell
CSFSnw	common source with improved load	time invariant	square	4.5 µm
CASFSnw	cascode with improved load	time invariant	square	4.5 µm
CSFLnw	common source with improved load	time invariant	L-shaped	19 µm
CASFLnw	cascode with improved load	time invariant	L-shaped	19 µm
CSTVFLnw	common source with improved load	time variant	L-shaped	19 µm
CSTVFlnw	common source with improved load	time variant	L-shaped	10 µm

Table 1: Detailed description of the circuits implemented in the test chip.

V. Simulation with Spectre

The designed layouts are simulated with Spectre, with parasitic capacitances extracted. The amplifier and CDS circuits are powered during 160 ns, which defines the pixel readout time. The integration time, or time between two successive pixel readouts, is 160 µs. The temperature is set to 20°C. The results of the simulation are presented in Table 2.

Design name	Input [µV/e]	Amplifier gain	SF gain	Column output [µV/e]	Noise rms [µV]	ENC [e]	Current [µA]
CSFSnw	6.2	14.5	0.7	64.0	590.5	9.2	4.1
CASFSnw	9.9	11.3	0.7	79.9	664.3	8.3	4.4
CSFLnw	2.6	15.4	0.7	28.2	625.0	22.2	5.8
CASFLnw	3.5	11.4	0.7	28.3	835.0	29.5	3.4
CSTVFLnw	2.7	10.3	0.7	20.2	530.0	26.2	24.3
CSTVFlnw	4.6	9.5	0.7	31.6	508.6	16.1	23.7

Table 2: The results of simulation of the circuits with Spectre.

VI. Charge collection efficiency simulation

The charge collection efficiency (CCE) is simulated with the device simulator ISE-TCAD for different sizes of the square nwell and the epitaxial layer thickness. Two ways of doping of the epitaxial layer are tested: uniformly doped and gradually doped (graded). In case of graded epi-layer the doping decreases in the nwell direction as power 10 of the distance. The entry position of minimum ionizing particle (m.i.p.) is uniformly distributed in the area of the central pixel (seed pixel) in a 5×5 pixels matrix. The collected charge is averaged over the m.i.p. entry

position and the charge collected in the seed pixel and in the clusters of 3×3 and 5×5 is calculated. The charge collection efficiency normalized to the total delivered charge by m.i.p. in the substrate is presented in Table 3.

epi-layer	epi thickness [μm]	Square Nwell size [μm]	CCE seed [%]	CCE cls3x3 [%]	CCE cls5x5 [%]	time for 90% collection in seed [ns]
uniform	20	2.4	5	14	21	198
uniform	14	2.4	8	22	32	190
uniform	8	2.4	18	48	60	134
uniform	20	4.5	15	46	63	167
uniform	14	4.5	22	62	80	139
uniform	8	4.5	35	78	87	74
graded	20	2.4	10	32	45	180
graded	14	2.4	14	40	53	160
graded	20	4.5	27	71	86	108
graded	14	4.5	31	74	85	36

Table 3: Charge collection efficiency in 5×5 pixels matrix simulated with ISE-TCAD for different substrates.

Design name	CCE seed [%]	CCE cls3x3 [%]	CCE cls5x5 [%]	Column output [μV/e]	Noise rms [μV]	ENC [e]	SNR
CSFSnw	16.1	56.0	64.9	57.6	783.6	13.6	19.4
CASFSnw	13.7	48.8	56.3	98.5	952.3	9.7	23.3
CSFLnw	34.4	88.6	91.4	24.5	893.1	36.4	15.5
CASFLnw	33.1	85.3	88.3	29.0	1015.3	35.0	15.5
CSTVFLnw	37.5	92.8	95.5	17.2	688.7	40.0	15.4
CSTVFlnw	26.7	80.2	86.9	25.4	670.0	26.4	16.6

Table 4: Charge collection measurements with ^{55}Fe source and measurements of the noise.

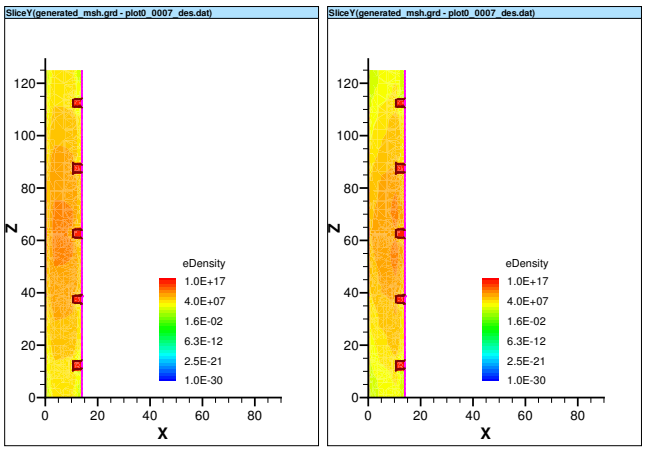

Figure 7: Electron concentration, in the p-substrate is due to energy deposited by m.i.p, shown after 19 ns: left not graded substrate, right graded substrate.

The influence of the graded substrate is shown in Figure 7, in the right: p doping gradually decreases in the positive x direction. The electrons concentration (after 19 ns of m.i.p. crossed the epitaxial layer) decreases slower in the case of uniformly doped substrate (Figure 7, left), and the spread will be larger. Thus, the charge collection efficiency is almost twice larger in case of a graded substrate.

VII. Measurements with ^{55}Fe source

The designed chip was tested with a X-Ray source of 5.9 keV. The pixel readout time is 160 ns, the integration time is 160 μs and the PCB temperature is stabilized at 20°C. The signal-to-noise ratio (SNR) is defined as the most probable value of the signal in the seed pixel divided by its noise. The results of the measurements are summarized in Table 4.

VIII. Conclusions

Few amplifier circuits and charge collecting diode layouts are proposed, designed and fabricated. The signal-to-noise ratio is maximized by optimizing transistor parameters for different size of charge collection diode.

The proposed amplifier schematics were tested with an ^{55}Fe source. The highest signal-to-noise ratio of 23 is obtained for improved cascode with feedback design and square nwell (4.5×4.5 μm^2). For the same square

nwell, the improved common source with feedback design shows smaller signal-to noise-ratio of 19, however, this schematic is more simple and more resistant to CMOS process variation.

The medium size of L-shaped nwell shows a signal-to noise ratio of about 17. For the large L-shaped diode, the amplifiers with time variant feedback and time invariant feedback have similar SNR of 15. The charge collection efficiency in the seed pixel can be improved by almost a factor of two by using an L-shaped nwell, but the signal-to-noise ratio decreases, due to capacitance increase.

The measured charge collection efficiency and the noise are in a good agreement with simulations with Spectre and ISE-TCAD.

The simulation of uniform and gradient doping of epitaxial layer was performed. For the same thickness, the graded epitaxial layer almost doubles the charge collection efficiency.

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REFERENCES

[1] R. Turchetta, J.D. Berst, B. Casadei, G. Claus, C. Colledani, W. Dulinski, Y. Hu, D. Husson, J.-P. Le Normand, J.-L. Riester, G. Deptuch, U. Goerlach, S. Higueret and M. Winter, A Monolithic Active Pixel Sensor for Charged Particle Tracking and Imaging Using Standard VLSI CMOS Technology Nuclear Instruments & Methods in Physics Research Section A 458 (2001) 677-689

[2] The Cadence Virtuoso Spectre Circuit Simulator, Cadence Design Systems, Inc.

[3] 1995-2004 ISE Integrated Systems Engineering AG, Switzerland.

[4] M.Winter et al., A Swift and Slim Flavour Tagger Exploiting the CMOS Sensor Technology, proceedings of the Linear Collider Workshop LCWS-05, Stanford, USA, March 2005.

[5] Andrei Dorokhov, NMOS-based high gain amplifier for MAPS. VIth International meeting on front end electronics for high energy, nuclear and space applications, Perugia, Italy 17- 20 May 2006