Data Flow of a Vertex Detector made of Fast Column // CMOS Sensors

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OUTLINE

• Major sources of the data flow :
  ✤ Beamstrahlung e±  ✤ Electronic noise ???

• Basic features of CMOS Vertex Detector geometry :
  ✤ Read-out time per layer  ✤ Assumed sensor read-out architecture

• Preliminary estimate of data flow

• Summary
Dominant source of hits: $e^\pm$ from Beamstrahlung

1st layer (L0): $\gtrsim 5 \text{ hits/cm}^2/\text{BX}$ for 4T / 500 GeV / $R_0 = 1.5 \text{ cm}$ / no safety factor

$\rightarrow \lesssim 1.8 \cdot 10^{12} \text{ e}^\pm/\text{cm}^2/\text{yr}$ (safety factor of 3)

- 2nd layer: 8 (6 ?) times less
- 3rd layer: 25 (< 20 ?) times less

Consequences on Occupancy in 1st layer (L0):

$\gtrsim 0.9 \%$ hit occupancy in 50 $\mu$s (r.o. time of TESLA TDR)

$\leftarrow$ signal spread on $\lesssim 4.5$–9 % pixels (cluster multiplicity $\sim 5$-10)

1) aim for shorter read-out time in L0 than in TDR $\iff$ typically $\lesssim 25 \mu$s

(compromise with power dissipation, multiple scattering, ...)

2) aim for shorter read-out time in L1 than in TDR $\iff$ typically $\sim 50 \mu$s (vs 250 $\mu$s)

and presumably smaller radius (e.g. $\sim 20$ – 22 mm)

(use tracks extrapolated from L1-4 down to L0)

3) aim for ”relaxed” read-out time in L2, L3, L4: $\sim 100$ – 200 $\mu$s (vs 250 $\mu$s)

$\leftarrow$ depends on backscattered $e^\pm$ rate
Consequences on Inner Layer Design

- $\lesssim 25 \, \mu s$ in L0:
  - columns of 256 pixels (20 $\mu m$ pitch) $\perp$ beam axes
  - read out in $\parallel$ at $\sim 10$ MHz $\rightarrow$ 5 mm depth

- $\sim 50 \, \mu s$ in L1:
  - columns of 512 pixels (25 $\mu m$ pitch) $\perp$ beam axes
  - read out in $\parallel$ at $\sim 10$ MHz $\rightarrow$ 13 mm depth

- $\lesssim 2$ mm wide side band hosting ADC, sparsification, ...
  - eliminate pixels with $\lesssim 3$ N

- Option with discriminator instead of ADC:
  - requires smaller pitch $\leftrightarrow$ presumably same data rate
Basic Vertex Detector Design features

- Geometry: 5 cylindrical layers (R = 15 – 60 mm), $\|\cos\theta\| \leq 0.90 – 0.96$ (possibly 6 layers)
- L0 and L1: fast col. // architecture
- L2, L3 and L4: possibly multi-memory pixel architecture (?)
- Pixel pitch varied from 20 $\mu m$ (L0) to 40 $\mu m$ (L4) by 5 $\mu m$ steps $\rightarrow$ minimise $P_{\text{diss}}$

<table>
<thead>
<tr>
<th>Layer</th>
<th>Radius (mm)</th>
<th>Pitch $\mu m$</th>
<th>$t_{r.o.}$ $\mu s$</th>
<th>$N_{\text{lad}}$</th>
<th>$N_{\text{pix}}$ $10^6$</th>
<th>$P_{\text{inst diss}}$ (W)</th>
<th>$P_{\text{mean diss}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>20</td>
<td>25</td>
<td>&lt;100</td>
<td>&lt;5</td>
</tr>
<tr>
<td>L1</td>
<td>25</td>
<td>25</td>
<td>50</td>
<td>26</td>
<td>65</td>
<td>&lt;130</td>
<td>&lt;7</td>
</tr>
<tr>
<td>L2</td>
<td>37</td>
<td>30</td>
<td>&lt;200</td>
<td>24</td>
<td>75</td>
<td>&lt;100</td>
<td>&lt;5</td>
</tr>
<tr>
<td>L3</td>
<td>48</td>
<td>35</td>
<td>&lt;200</td>
<td>32</td>
<td>70</td>
<td>&lt;110</td>
<td>&lt;6</td>
</tr>
<tr>
<td>L4</td>
<td>60</td>
<td>40</td>
<td>&lt;200</td>
<td>40</td>
<td>70</td>
<td>&lt;125</td>
<td>&lt;6</td>
</tr>
<tr>
<td>Total</td>
<td>142</td>
<td>305</td>
<td>&lt;565</td>
<td></td>
<td></td>
<td>&lt;3–30</td>
<td></td>
</tr>
</tbody>
</table>

- Ultra thin layers: $\lesssim 0.2 \% X_0$/layer (extrapolated from STAR-HFT; 35 $\mu m$ thick sensors)
- Very low $P_{\text{mean diss}}$: $<< 100$ W (exact value depends on duty cycle)
- Fake hit rate $\lesssim 10^{-5} \rightarrow$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)
■ Raw data flow (in absence of any signal):

\[ L_0 : \sim 25 \text{ Mpixels read 40 times / train} \cong 1 \text{ Gpixels / train} \]
\[ L_1 : \sim 50 \text{ MPixels read 20 times / train} \cong 1 \text{ Gpixels / train} \]
\[ L_2 + L_3 + L_4 : \lesssim 300 \text{ Mpixels read } \lesssim 10 \text{ times /train} \cong 3 \text{ Gpixels / train} \]

Total \( \cong 5 \text{ Gpixels / train} \mapsto 25 \text{ Gpixels / s} \)

\[ 3 \text{ Bytes/pixel (} \leq 20 \text{ address bits + 5–4 charge bits)} \Rightarrow \text{ raw data flow } \cong 75 \text{ GB / s} \]

■ Signal data size dominated by \( e_{BS}^\pm \): \( \gtrsim 10^3 \text{ hits / BX} \mapsto 3 \cdot 10^6 \text{ hits / train} \)

\[ \cong \text{ Assuming 5 pixels / cluster : } 15 \cdot 10^6 \text{ pix/train} \mapsto 45 \text{ MB / train} \]
\[ \cong \text{ Uncertainties on beamstrahlung rate prediction (factor 3 - 5) } \mapsto 135–225 \text{ MB / train} \Rightarrow 0.7–1.1 \text{ GB / s} \]

■ Efficiency vs rate of fake clusters

studied on real (MIMOSA-9) beam test data:

\[ \cong \text{ vary cut on seed pixel : } 6 \mapsto 12 \text{ ADC units (N } \sim 1.5 \text{ unit)} \]
\[ \cong \text{ vary cut on } \Sigma \text{ of crown charge : } 0, 3, 4, 9, 13, 17 \text{ ADC units} \]
\[ \Rightarrow \epsilon_{det} \sim 99.9 \% \text{ for fake rate } \sim 10^{-4} – 10^{-5} \]
\[ \Rightarrow \text{ Electronic noise } \lesssim 1 – 10 \text{ MB / s after sparsification} \mapsto \text{ negligible} \]
Vertex Detector data flow dominated by Beamstrahlung electrons
  $\Rightarrow$ rate known within factor of 3–5

Electronic noise of CMOS sensors expected to add $< 1\%$ data flow to $e^{\pm}_{BS}$ hits
  (based on sensor prototype tests)

Whole detector data flow expected to amount to $\sim 0.2$ to $1$ GB/s
  (depending on $e^{\pm}_{BS}$ rate)

Pending question: can part of the $e^{\pm}_{BS}$ hits be eliminated upstream of central DAS?
- Adapting the Inner Most Layer to High Background

- Design inner most layer (L0) to minimise its sensitivity to (unexpected) high occupancy (> 10%)

- Double sided layer → ∼ 1 mm long mini-vectors connecting impacts on both sides of layer

  ▶ Needs a detailed feasibility (engineering) study ....