Data Flow of a Vertex Detector made of Fast Column // CMOS Sensors

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OUTLINE

- Major sources of the data flow :
  - Beamstrahlung $e^{\pm}$
  - Electronic noise ???
- Basic features of CMOS Vertex Detector geometry :
  - Read-out time per layer
  - Assumed sensor read-out architecture
- Preliminary estimate of data flow
- Summary

Constraints from Beamstrahlung

- Dominant source of hits : $e^{\pm}$ from Beamstrahlung

- 1st layer (L0) : $\gtrsim$ 5 hits/cm^2/BX for 4T / 500 GeV / R_0 = 1.5 cm / no safety factor
  $\rightarrowtail \lesssim 1.8 \cdot 10^{12}$ $e^{\pm}$/cm^2/yr (safety factor of 3)
  - 2nd layer: 8 (6 ?) times less
  - 3rd layer: 25 ($<$ 20 ?) times less

- Consequences on Occupancy in 1st layer (L0) : $\lesssim$ 0.9 % hit occupancy in 50 μs (r.o. time of TESLA TDR)
  $\hookrightarrow$ signal spread on $\lesssim$ 4.5–9 % pixels (cluster multiplicity $\sim$ 5-10)

  $\Rrightarrow$ 1) aim for shorter read-out time in L0 than in TDR $\rightarrowtail$ typically $\lesssim$ 25 μs
  (compromise with power dissipation, multiple scattering, ...)

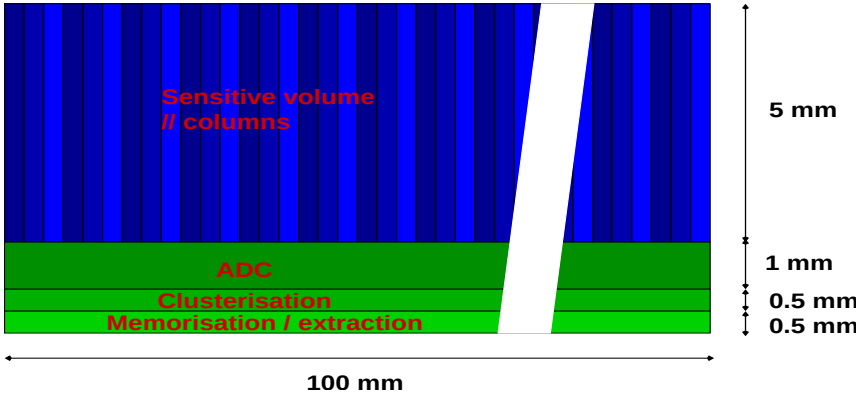
  2) aim for shorter read-out time in L1 than in TDR $\rightarrowtail$ typically $\sim$ 50 μs (vs 250 μs)
  and presumably smaller radius (e.g. $\sim$ 20 – 22 mm)
  (use tracks extrapolated from L1-4 down to L0)

  3) aim for "relaxed" read-out time in L2, L3, L4: $\sim$ 100 – 200 μs (vs 250 μs)
  $\hookrightarrow$ depends on backscattered $e^{\pm}$ rate

Consequences on Inner Layer Design

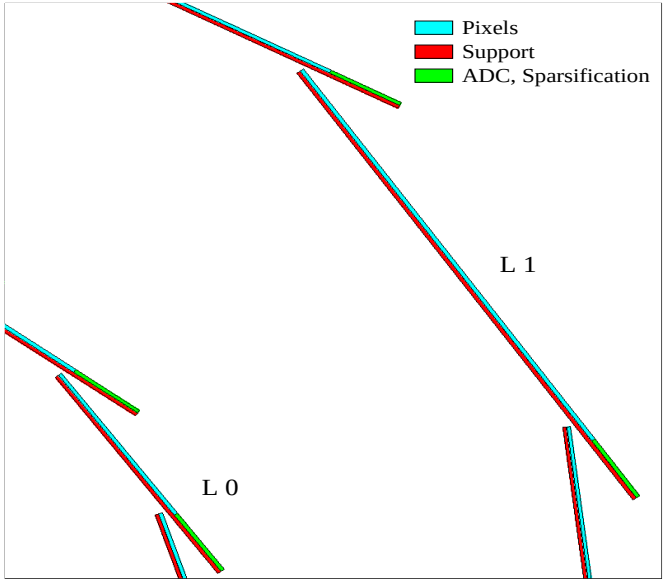
- $\lesssim$ 25 μs in L0:
  columns of 256 pixels (20 μm pitch) $\perp$ beam axes
  read out in // at $\sim$ 10 MHz $\longrightarrow$ 5 mm depth

- $\sim$ 50 μs in L1:
  columns of 512 pixels (25 μm pitch) $\perp$ beam axes
  read out in // at $\sim$ 10 MHz $\longrightarrow$ 13 mm depth



- $\lesssim$ 2 mm wide side band hosting ADC, sparsification, ...
  $\hookrightarrow$ eliminate pixels with $\lesssim$ 3 N

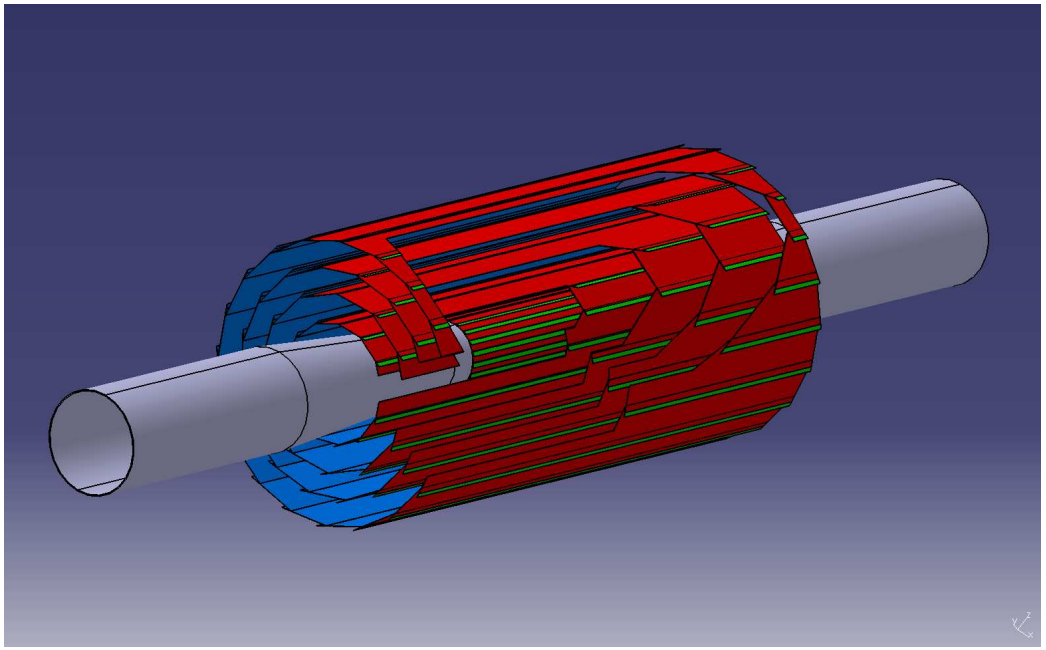
- Option with discriminator instead of ADC :
  requires smaller pitch $\rightarrowtail$ presumably same data rate



Basic Vertex Detector Design features

- Geometry : 5 cylindrical layers (R = 15 – 60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96 (possibly 6 layers)
- L0 and L1 : fast col. // architecture
- L2, L3 and L4 : possibly multi-memory pixel architecture (?)
- Pixel pitch varied from 20 μm (L0) to 40 μm (L4) by 5 μm steps $\rightarrowtail$ minimise P_{diss}

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	20	25	$<$100	$<$5
L1	$\leq$ 25	25	50	$\leq$26	$\leq$ 65	$<$130	$<$7
L2	37	30	$<$200	24	75	$<$100	$<$5
L3	48	35	$<$200	32	70	$<$110	$<$6
L4	60	40	$<$200	40	70	$<$125	$<$6
Total				142	**305**	$<$565	$<$3–30



- Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; 35 μm thick sensors)
- Very low P_{diss}^{mean}: $<<$ 100 W (exact value depends on duty cycle)
- Fake hit rate $\lesssim 10^{-5} \rightarrowtail$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)

Vertex Detector Data Flow

- **Raw data flow (in absence of any signal):**
  - L0 : $\sim$ 25 Mpixels read 40 times / train $\cong$ 1 Gpixels / train
  - L1 : $\sim$ 50 MPixels read 20 times / train $\cong$ 1 Gpixels / train
  - L2 + L3 + L4 : $\lesssim$ 300 Mpixels read $\lesssim$ 10 times /train $\cong$ 3 Gpixels / train

    Total $\cong$ 5 Gpixels / train $\mapsto$ 25 Gpixels / s
  - 3 Bytes / pixel ($\leq$ 20 address bits + 5–4 charge bits) $\Rightarrow$ **raw data flow $\cong$ 75 GB / s**

- **Signal data size dominated by $e^{\pm}_{BS}$:** $\gtrsim 10^3$ hits / BX $\mapsto$ $3 \cdot 10^6$ hits / train
  - Assuming 5 pixels / cluster : $15 \cdot 10^6$ pix / train $\mapsto$ 45 MB / train
  - Uncertainties on beamstrahlung rate prediction (factor 3 - 5) $\mapsto$ 135–225 MB / train $\Rightarrow$ 0.7–1.1 GB / s

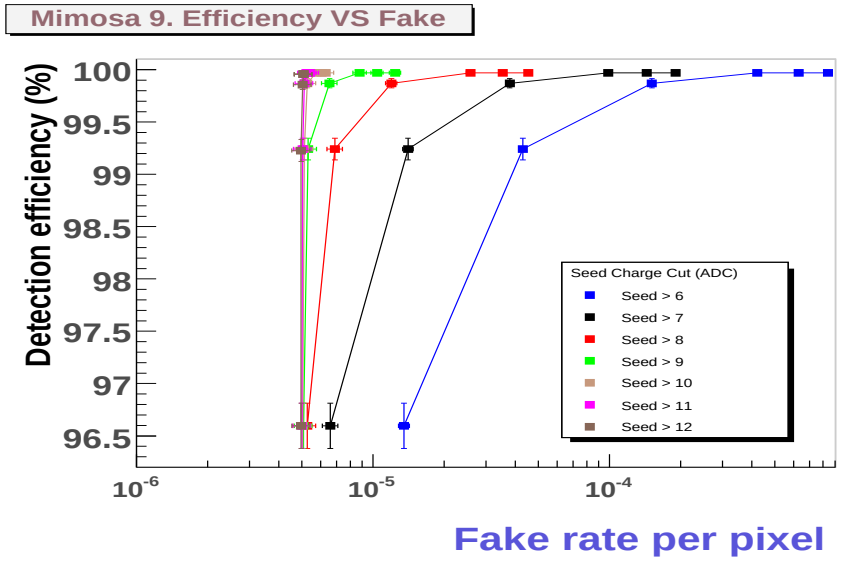
- **Efficiency vs rate of fake clusters**

  studied on real (MIMOSA-9) beam test data:
  - vary cut on seed pixel : 6 $\rightarrowtail$ 12 ADC units (N $\sim$ 1.5 unit)
  - vary cut on Σ of crown charge : 0, 3, 4, 9, 13, 17 ADC units

    $\Rightarrow \epsilon_{det} \sim$ 99.9 % for fake rate $\sim 10^{-4}$ – 10^{-5}

    $\Rightarrow$ Electronic noise $\lesssim$ 1 – 10 MB / s after sparsification

    $\hookrightarrow$ negligible



Summary & Conclusion

- **Vertex Detector data flow dominated by Beamstrahlung electrons**

  $\longmapsto$ **rate known within factor of 3–5**

- **Electronic noise of CMOS sensors expected to add $<$ 1 % data flow to $e^{\pm}_{BS}$ hits**

  (based on sensor prototype tests)

- **Whole detector data flow expected to amount to $\sim$ 0.2 to 1 GB / s**

  (depending on $e^{\pm}_{BS}$ rate)

- **Pending question : can part of the $e^{\pm}_{BS}$ hits be eliminated upstream of central DAS ?**

Adapting the Inner Most Layer to High Background

- Design inner most layer (L0) to minimise its sensitivity to (unexpected) high occupancy ($\gtrsim$ 10 %)
- Double sided layer $\rightarrowtail \sim$ 1 mm long mini-vectors connecting impacts on both sides of layer
  - ▷ Needs a detailed feasibility (engineering) study ....