



Towards a 10 μ s, thin high resolution pixelated CMOS sensor system for future vertex detectors

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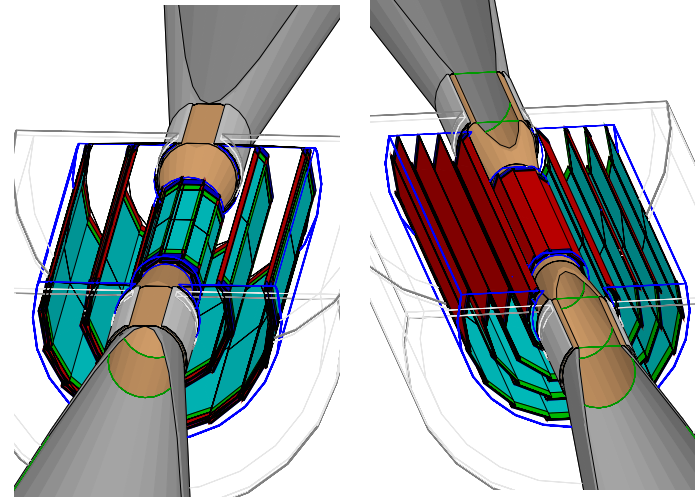
On behalf of the IPHC-IRFU collaboration

- Physics motivations.
- Principle of operation and performances.
- MIMOSA-26 and its applications.
- System integration.
- Developments.
- Summary and conclusions.

A vertex detector for the ILC

Two alternative geometries

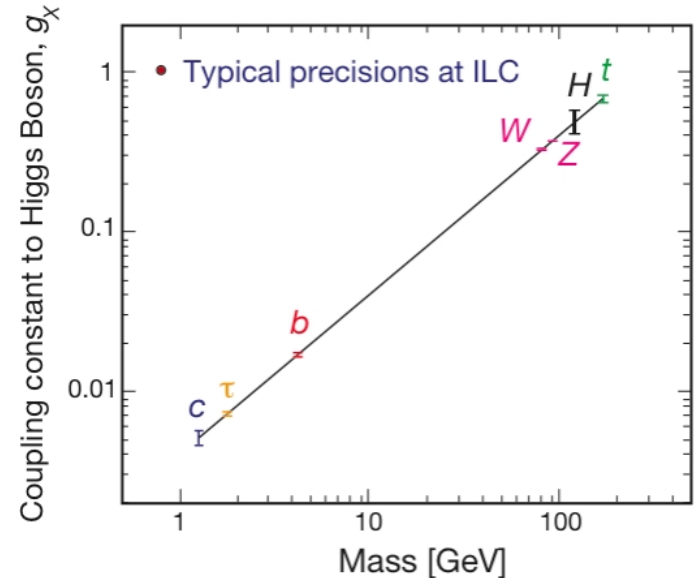
- 5 single-sided layers.
- 3 double-sided layers.



Sensor requirements

- Single point resolution $\sim 3\mu\text{m}$.
- Material budget $0.16/0.11\% X_0/\text{layer}$.
- Integration time $25 - 100 \mu\text{s}$.
- Radiation tolerance $\sim 0.3\text{MRad}$, few $10^{11}n_{\text{eq}}/\text{cm}^2$.
- Averaged power dissipated $\ll 100 \text{ W}$.

$$\sigma_{\text{IP}} = a \oplus b/p\sin^{3/2}\theta$$
$$a \leq 5\mu\text{m}, b \leq 10\mu\text{m GeV}$$
$$(a = 12\mu\text{m}, b = 70\mu\text{m GeV @ LHC})$$



CMOS sensor principle

Signal collection

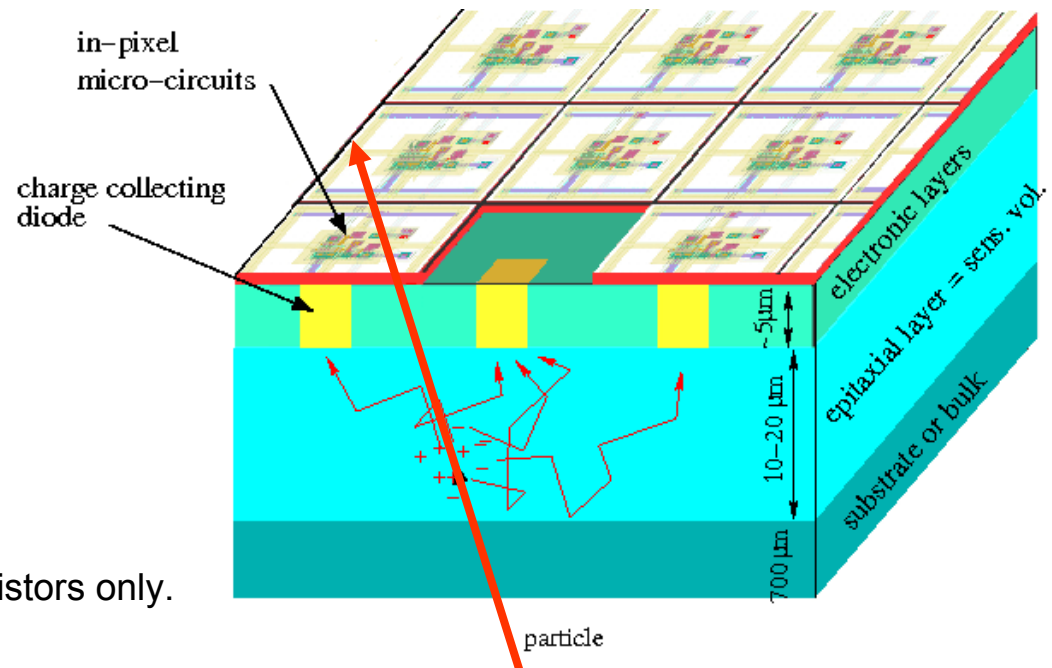
- Charges generated in epitaxial layer \rightarrow $\sim 1000 e^-$ for MIP.
- Charge carriers propagate thermally.
- In-pixel charge to signal conversion.

Advantages

- High granularity.
- Thickness ($\sim O(50\mu\text{m})$).
- Integrated signal processing.

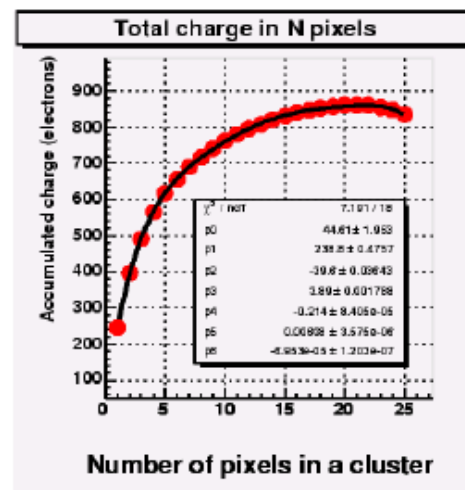
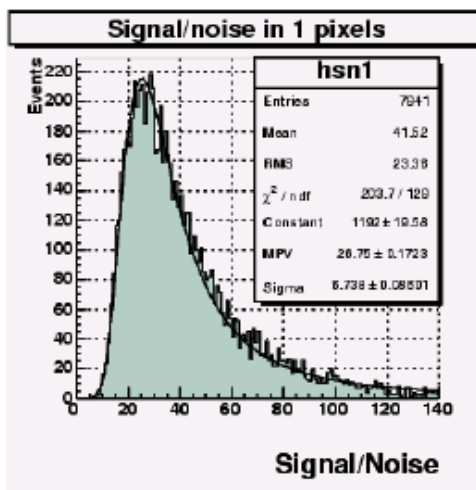
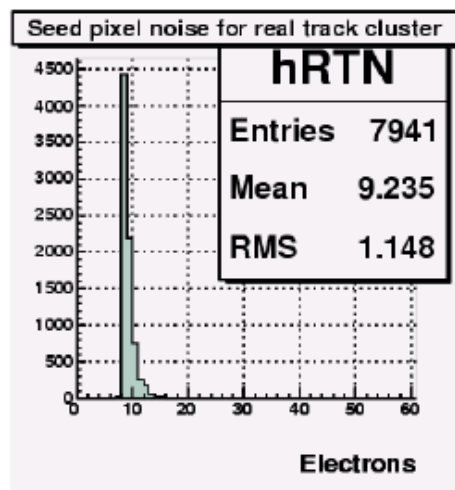
Issues

- Undepleted volume limitations .
 - radiation tolerance.
 - intrinsic speed.
- Small signal $O(100e^-)$ /pixel.
- In-pixel μ -circuits with NMOS transistors only.



Basic performances

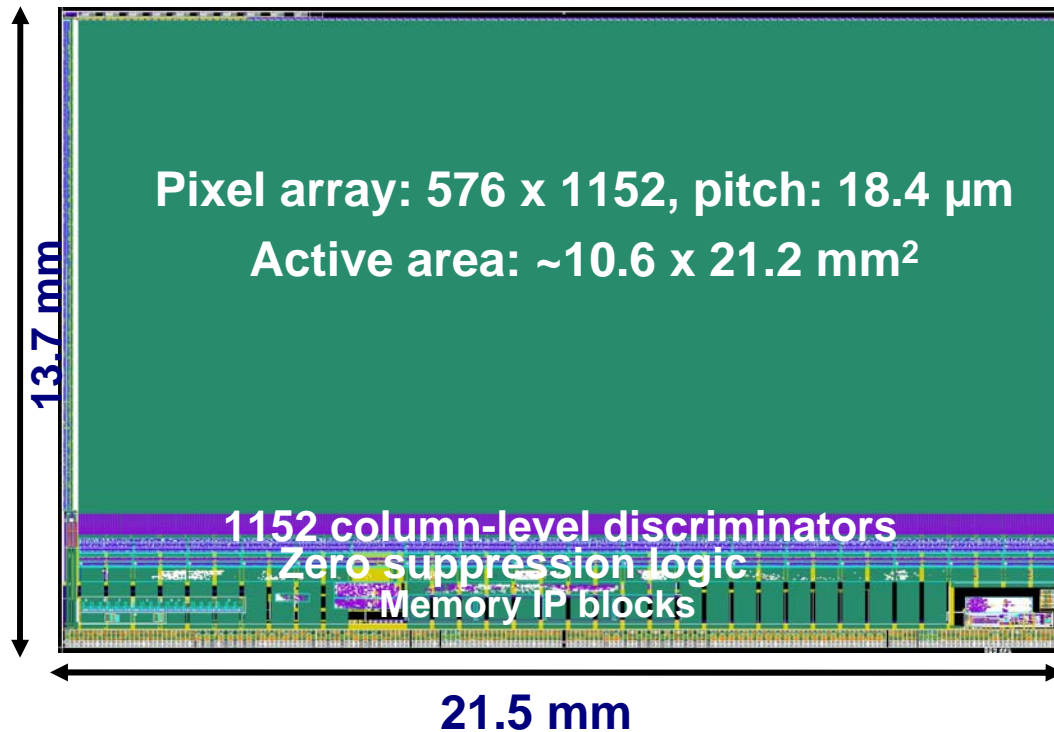
- More than 30 different sensors designed, fabricated and tested (lab & beam).
- Extensive use of $0.35\mu\text{m}$ CMOS technology.
- Room temperature operation.
- Noise $\sim 10\text{-}15e^-$.
- S/N $\sim 15\text{-}30$.
- Detection efficiency $\sim 100\%$ @ fake hit rate $O(10^{-4} - 10^{-5})$.
- Radiation tol. $> 1\text{MRad}$ and $10^{13}n_{\text{eq}}/\text{cm}^2$ with $10\mu\text{m}$ pitch ($2 \times 10^{12}n_{\text{eq}}/\text{cm}^2$ with $20\mu\text{m}$ pitch).
- Spatial resolution $1\text{-}5\mu\text{m}$ (pitch and charge-encoding dependent).
- Macroscopic sensors (Ex. MIMOSA-5: $1.7 \times 1.7\text{ mm}^2$, 10^6 pixels).
- Used in beam telescopes and VTX demonstrators (EUNET, TAPI, STAR, CBM).



Mimosa-26

Fast full scale sensors: ~10kFrame/s

column parallel architecture + integrated zero-suppression
(prototyping with MIMOSA-22 for binary output + SUZE-01 for \emptyset)



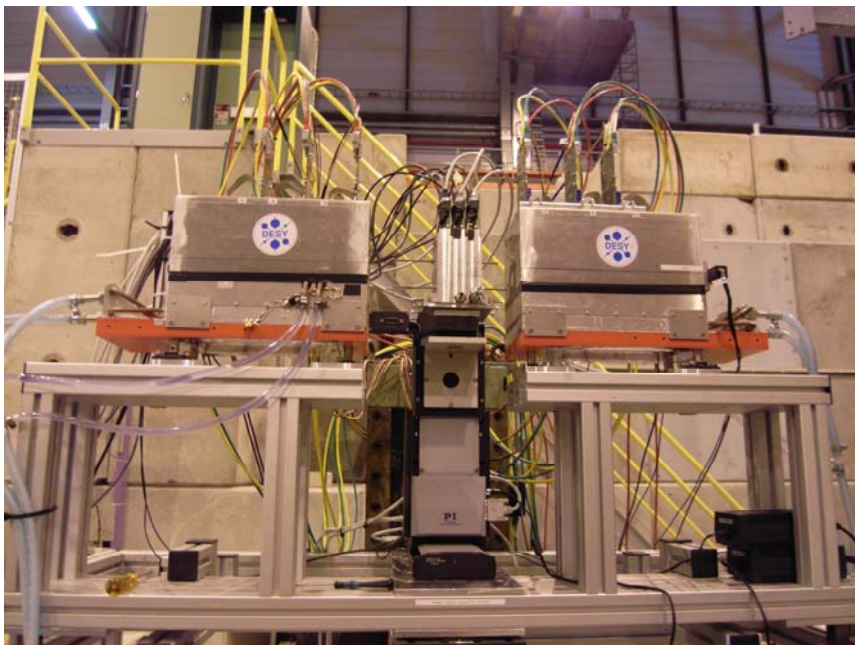
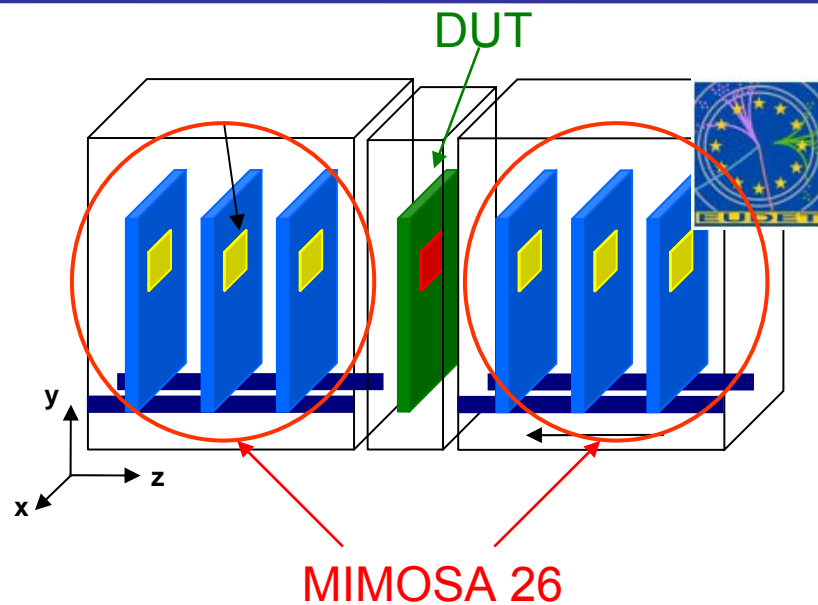
- Active area ~2 cm^2 .
- 0.35 μm technology.
- Binary output (3.5 - 4 μm spatial resolution).
- In-pixel CDS + preamp.
- Column level discrimination.
- Power dissipated ~280 mW/cm^2 (rolling shutter).
- Integration time ~100 μs .

It was tested extensively in the laboratory: performances as expected

EUDET beam telescope

Reference planes of EUDET Beam Telescope

- Supported by EU FP6.
- Infrastructure to support the ILC detector R&D.
- Specifications:
 - Extrapolated resolution $< 2 \mu\text{m}$.
 - Sensor area $\sim 2 \text{ cm}^2$.
 - Read-out speed $\sim 10 \text{ kframe/s}$.
 - Up to 10^6 hits/s/cm^2 .



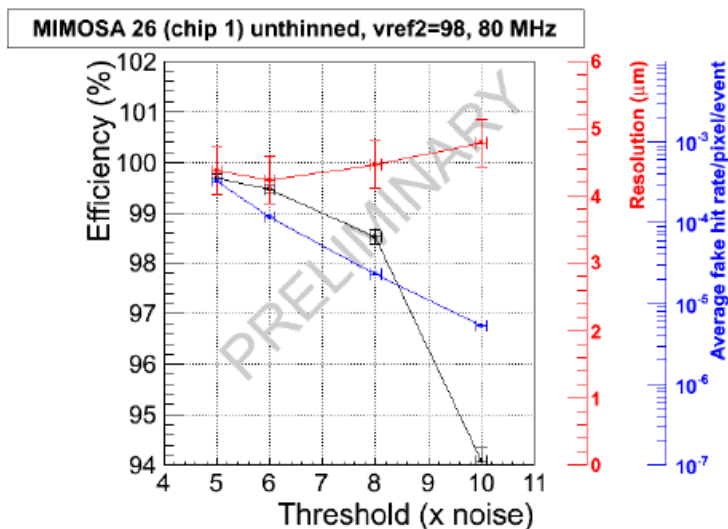
Commissioning @ CERN-SPS last year:

- BT completely equipped with MIMOSA-26.
- Residuals compatible with $\sigma = 4 \mu\text{m}$.

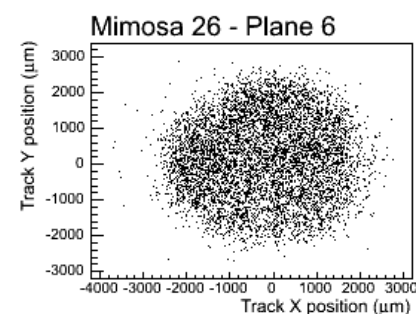
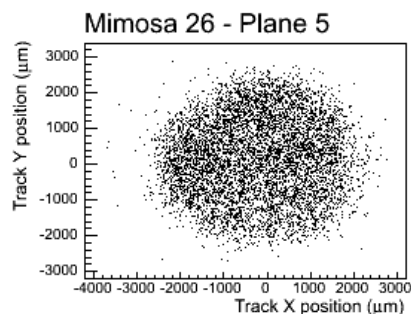
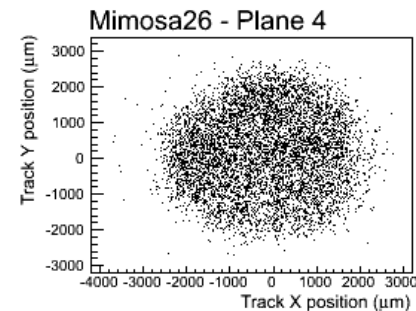
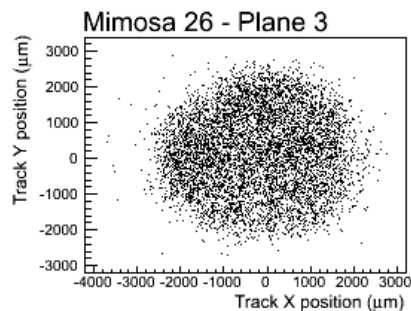
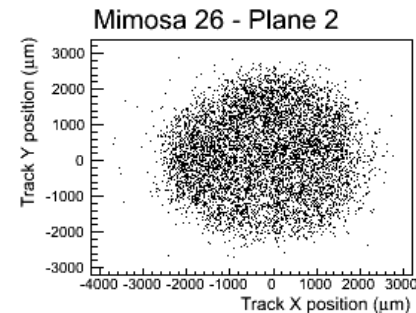
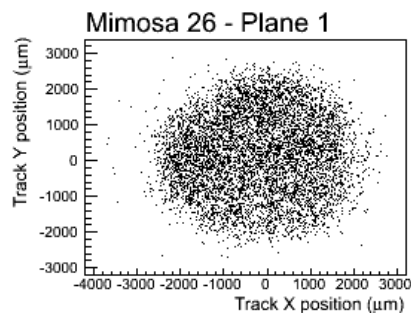
www.eudet.org

Preliminary beam test results

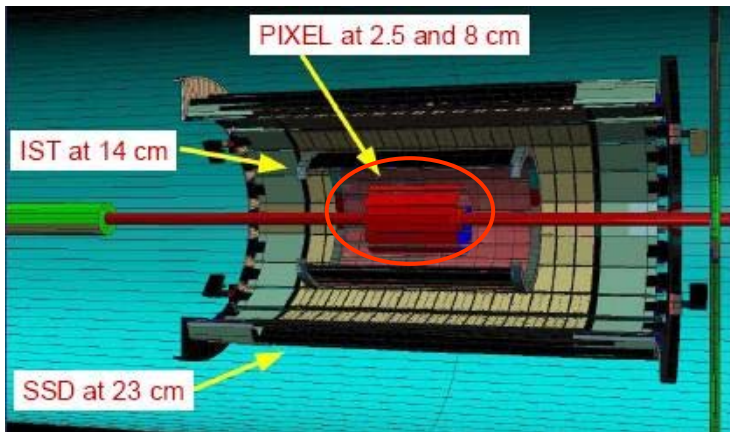
- TAPI = IPHC-Strasbourg BT for MIMOSA development.
- Test @ CERN-SPS (120 GeV π^- beam).
- 6 MIMOSA-26 sensors running simultaneously at nominal speed (80 MHz).
- 3×10^6 triggers.



$\epsilon = 99.5 \pm 0.1$ (stat.) ± 0.3 (prel.) %
@ fake hit rate $O(10^{-4})$



Mimosa-26 architecture: evolutions

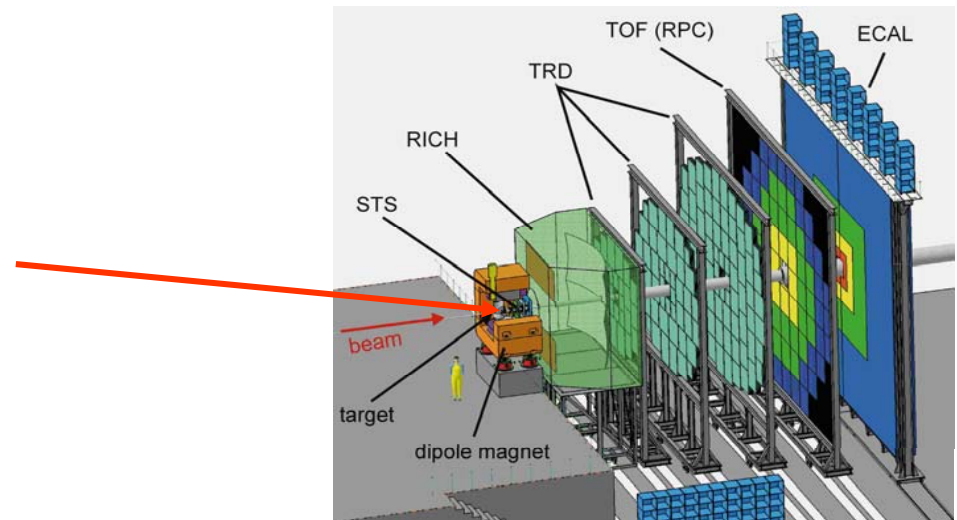


STAR @ RHIC Heavy Flavour Tracker

- 1152 x 1024 pixels; 200 μ s integration time.
- Improved radiation tolerance.
- Submission late 2010.
- First data in 2013.

CBM @ FAIR Micro Vertex Detector

- Double sided readout.
- 0.18 μ m (40 \rightarrow 20 μ s integration time).
- Prototyping until 2012.



Interest expressed by the ALICE collaboration for the upgrade in view of sLHC

The ILD applications

Physics requirements

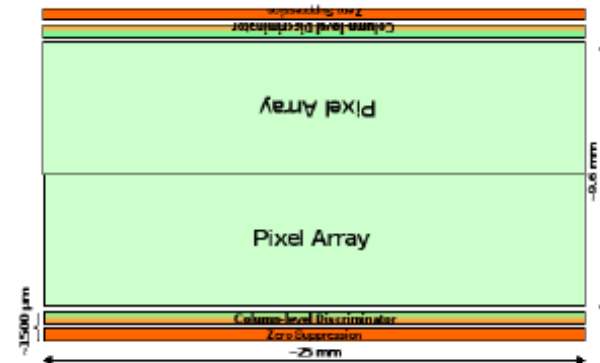
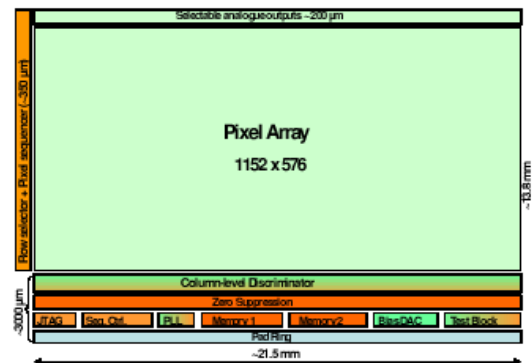
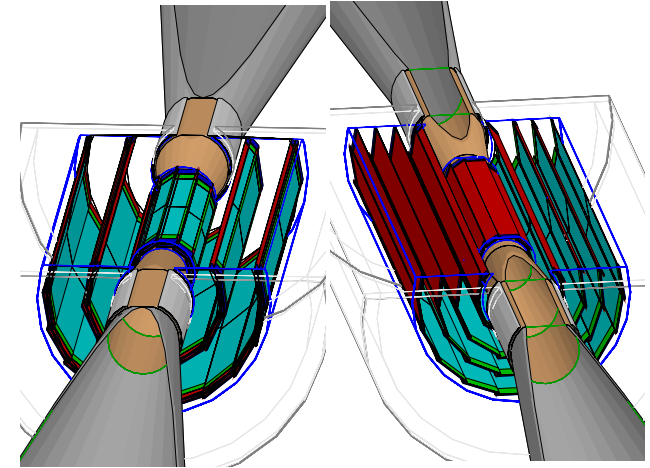
- single point resolution $\sim 3\mu\text{m}$.
- integration time 25 – 100 μs .
- ...

Extension for the outer VTX layers:

- $\sigma \sim 3\mu\text{m}$: 4-5 bits ADC and a $\sim 35\mu\text{m}$ pitch (r.o. $\sim 100\mu\text{s}$).

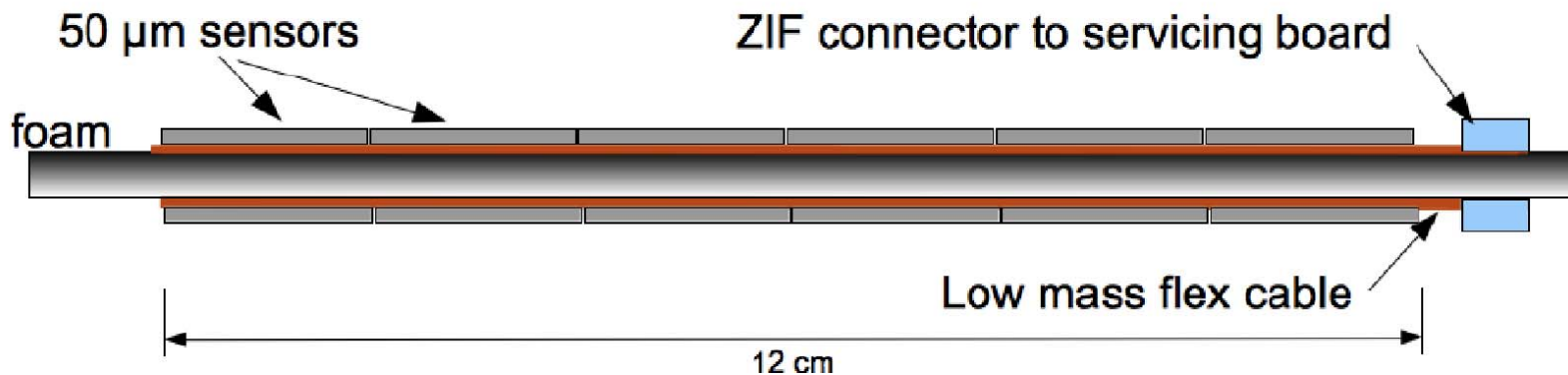
For the inner layers:

- $\sim 15\mu\text{m}$ pitch \rightarrow binary readout.
- Double-sided r.o. \rightarrow r.o. $\sim 50\mu\text{s}$.
- Smaller feature size $\rightarrow 35 - 40\mu\text{s}$.
- Double sided ladders $\rightarrow \ll 35\mu\text{s}$.



System integration: the PLUME project

- Pixel Ladder with **U**ltra-low **M**aterial **E**mbedding.
- Bristol - DESY - Oxford - Strasbourg.
- Double sided ladder equipped with 2x6 MIMOSA-26 (ILC DBD 2012).
- 0.2 - 0.3 % X_0 .
- Explore feasibility, performances and added value of double-sided ladders.
- Allows for improved time resolution (outer layer with longer and fewer pixels).
- First prototype (reduced scale) tested at CERN-SPS last November.
- Double sided ladder prototype expected in 2012.
- Use of infrastructures foreseen in AIDA (FP7 project in preparation).



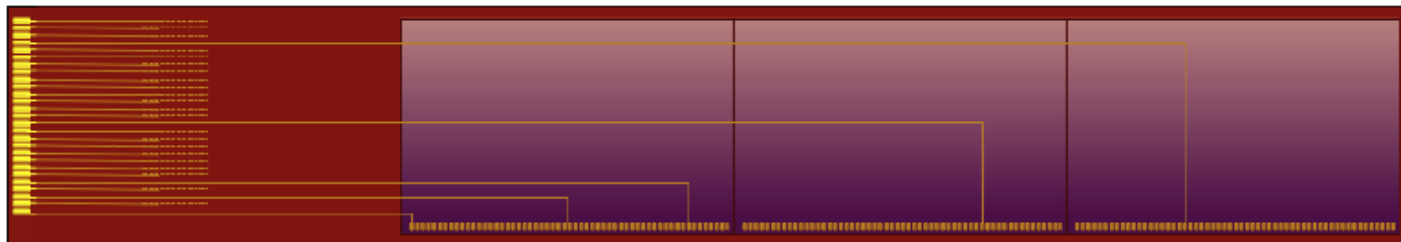
System integration: SERWIETE

- **SEnsor Row Wrapped In Extra-Thin Envelope** (HP 2 Project).
- Frankfurt – Darmstadt – Strasbourg.
- Sensors wrapped in thin polymerised film.
- $<0.15\%$ X_0 expected for sensor (35 μm thin) \oplus flex \oplus film (no mechanical support).
- May match cylindrical surfaces.
- Proof of principle in 2012.

Proto 1 ▷ Spring 2010



Proto 2 ▷ Summer 2011



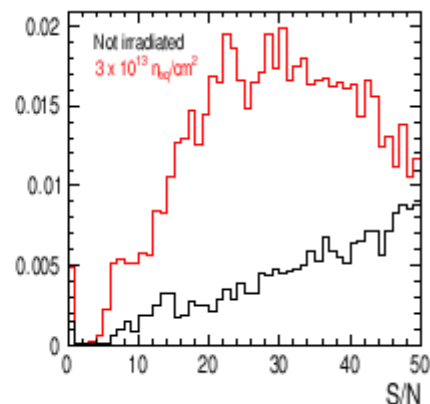
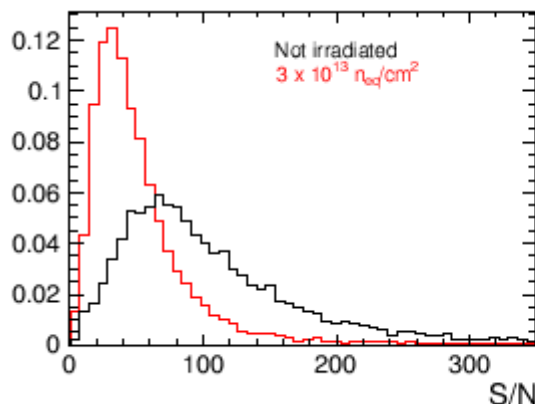
Further developments: high resistivity epi layer

High resistivity epitaxial layer ($O(10^3) \Omega \cdot \text{cm}$) \Rightarrow depleted sensitive volume!

- Faster readout.
- Improved radiation tolerance.

Exploration of the technology: MIMOSA-25 ($0.6 \mu\text{m}$)

- Fabricated in 2008 and tested at CERN-SPS before and after irradiation.
- Cluster size $\sim 2 \times 2$ pixels (3×3 for low resistivity epi-layer).
- S/N ~ 60 for seed (20-25 for low resistivity epi-layer - $\sim 30 @ 3 \cdot 10^{13} n_{\text{eq}}/\text{cm}^2$).
- $\varepsilon = 99.9\%$ ($99.5\% @ 3 \cdot 10^{13} n_{\text{eq}}/\text{cm}^2$).
- Improved tolerance to non-ionizing radiation (1-2 OoM).

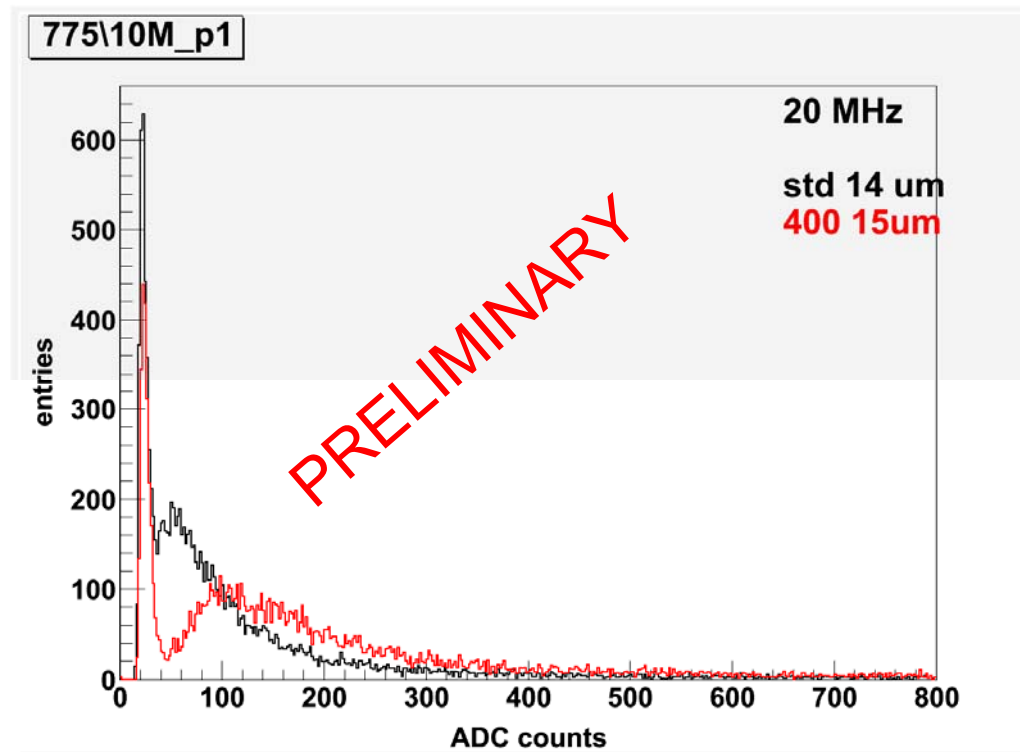


New VDSM technology under study in collaboration with CERN for sLHC

MIMOSA-26 with high resistivity epi layer

NEW!

MIMOSA-26 high res. (400 Ω -cm) 0.35 μ m presently under test (for STAR-HFT)



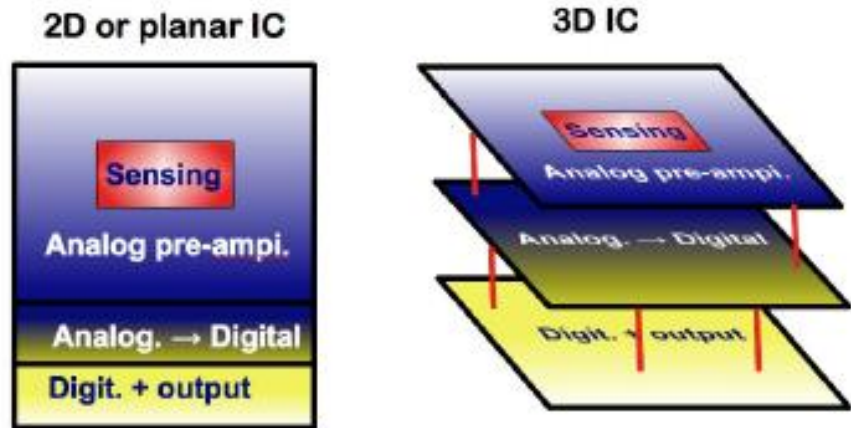
Further developments: 3D

Benefits:

- Increase integrated processing.
- 100% sensitive area.
- Select best process per layer task.

To be assessed:

- Material budget?
- Power dissipation?



Example

- Tier1: charge collection.
- Tier2: analog signal processing.
- Tier3: digital signal processing.
- Tier4: data transfer.

FNAL + IN2P3 + INFN + ... consortium (3DIC)

First chips (2-Tier 130nm technology) being fabricated

Summary and future perspectives

Current CMOS sensors

- Mature technology for real scale applications.
- High resolution, very low material budget.

First full scale sensor with high read-out speed: MIMOSA-26.

- Binary output + integrated zero-suppression.
- Tested in laboratory and on beam.
- EUDET-BT, STAR-HFT, ALICE tracker, CBM-MVD, ILD-VTX (option).

System integration studies started: PLUME, SERWIETE, → Material budget $\ll 0.5 \% X_0$

New perspectives

Depleted sensitive volume:

- Technology prototyped with MIMOSA-25.
- MIMOSA-26 high res. under test.
- Expectations: fast charge collection and non ionizing radiation tolerance $> 10^{14} n_{eq}/cm^2$.

3D integration technology:

- 4 CAIRN prototypes being produced (low power, few μs r.o., delayed readout with timestamp).
- Heterogeneous chip (depleted sensitive volume).

More information on

<http://www.iphc.cnrs.fr/-CMOS-ILC-.html>