Master Sciences – Mention Physique
Spécialité "Micro- Nano-Electronique"
2007/2008

Proposition de stage

Design and Realization of Integrated Structures to Test Analog and Digital Very Large Scale Integrated Circuits

Responsables du stage :

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A. Sujet bibliographique :
Testing complex integrated circuits (i.e. memories and microprocessors) is approached in automatic way to quickly check if the microchip can be used or discarded. The study of the current solutions and industrial implementations in scientific literature is a good starting point to evaluate the current state-of-the-art and search algorithms, procedures and circuits which can be successfully implemented in testing microchips for the particles physics. The investigation might be extended not only to test "go/no-go" functionality but also to provide more information about the status of the circuit, even during the normal functioning.

B. Description du stage :
During the test of ASICs it is common practice to use Automatic Test Equipments: the microchip is connected to a custom hardware/software which is able to analyze if the DC and AC parameters are within the design specifications. The implementation of test structures on-chip allows to characterize the internal circuits without the special hardware and drastically reduces connection to the external, with the exception of a limited number of pins and low-speed data exchange.

Electronics for High-Energy Physics experiments and in particular ASICs operate in a harsh environment due to ionizing particles which progressively degrade the devices. A well implemented Built-In Self Test (BIST) strategy helps a lot in screening the best chips by providing a quick answer "go/no-go" at the start-up and moreover by analyzing the variations and providing further information on the current status of the circuit and its performance.

Development of advanced BISTs started with large memories but nowadays it is a common practice to include in almost all digital systems, nevertheless using BISTs is getting more and more relevant in analog circuits as well as in mixed mode circuits (ADCs and DACs). The stage proposal aims to design and implement digital BISTs to characterize and test analogue blocks parameters (rising time, following time, jitter and mutual delay between pins) as well as digital BIST with advanced conceptions to execute tests both off-line (during dead time or pauses in normal functioning) and off-line (concurrent with the normal operations). The implementation will optimize the impact in terms of extra pins, area overhead and power consumption.

Using a CAD environment it will be possible to follow the design flow steps, starting from the simulation of the circuits either for analog or digital applications, and then integrating the blocks on silicon (layout) in order to create a reusable library of macroblocks which can be included in ASICs projects.

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