Internship 2008/2009

Design of a Full-Custom CMOS XFAB 0.18 µm Front-End Readout Chip for Photo-detector based on Planacon.

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A. Bibliographical review:

The bibliographical study concernes the state of the art of different front-end readout channel used in experimental subatomic physics, especially the low-noise preamplifier architecture implemented for Planacon readout channel.

B. Intership description :

Today, the main challenge of Positron Emission Tomography (PET) systems dedicated to small animal imaging is to obtain high detection efficiency and a highly accurate localization of radioisotopes. If we focus only on the PET characteristics such as the spatial resolution, its accuracy depends on the design of detector and on the electronics readout system as well. The design of such readout system with full custom submicrometer CMOS implementation consists of two main blocks from which the energy information and the time stamp with subnanosecond resolution can be obtained.

In our PET system design, a matrix of LYSO crystals has to be read at each end by a 1024 channels multi-anodes Planacon. A specific readout electronic is being developed at the Hubert Curien Multidisciplinary Institute (IPHC, France). The architecture of this readout for the energy information detection is composed of a low-noise preamplifier, a CR-RC shaper and an analogue memory. In order to obtain the required dynamic range from 16fC to 104 pC with good linearity, a current mode approach has been chosen for the preamplifier. To detect the signal with a temporal resolution of 1 ns, a comparator with a very low threshold (0.3 photoelectron) will be implement. It gives the time reference of arrival signal coming from the detector. In order to obtain the time coincidence with a temporal resolution of 1 ns, a Time-to-Digital Converter (TDC) based on a Delay-Locked-Loop (DLL) will be designed. The chip will be fabricated with XFAB 0.18 µm process.

In this context, the student will consider, according to his supervisor, the feasibility of the proposed architecture and design a demonstrator in CMOS XFAB 0.18 micron. To do this, the student will work with the Cadence analog design flow (Simulation→design verification).

Supervisory authority

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