

***Circuit-level power optimization for the digital blocks in
Monolithic Active Pixel Sensors (MAPS)***

Responsables du stage :

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A. Sujet bibliographique :

The properties of MAPS [1], especially being exposed to irradiation, degrade with the temperature increase. The sensitive volume of MAPS is placed on the same chip with digital electronics. Therefore, reduction of the power consumption of the digital blocks is an important issue for MAPS. There many different technique to reduce the power consumption: power gating, voltage scaling, voltage islands, proper transistor sizing.

B. Description du stage :

Investigate possible ways of reducing power consumption of the digital blocks to be used in MAPS.

The speed and the slope of digital controlling pulses provided by the standard CMOS logic cells for MAPS can be adjusted for the needs of pixel cell. Standard CMOS logic cell provides general fast pulse (<0.1ns), however, for some pixel cell configurations [2] one need rising edge fast and falling edge can be (or even required) few times slower.

The standard digital voltage for some controlling pulses can be reduced, as it is needed to control switches, working at low voltage and small swing. Therefore there is a room for the power reduction of the standard digital cells (such as gates, shift registers and memory cells) , and the aim is to design digital cells which has reduced short circuit-circuit power component, reduced digital voltage and have performances still acceptable for MAPS.

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- [2] A. Dorokhov, Optimization of amplifiers for MAPS, Topical workshop on electronics for particle physics, Prague, 3-7 September 2007