MimoTEL
User Manual

C. Colledani, W. Dulinski, H. Himmi, Ch. Hu, I.Valin
Institut de Recherches Subatomiques
IN2P3-CNRS / ULP Strasbourg – France

Document history		
Version	Date	Description
1.0	October 2006	Based on MimoStar2 Version

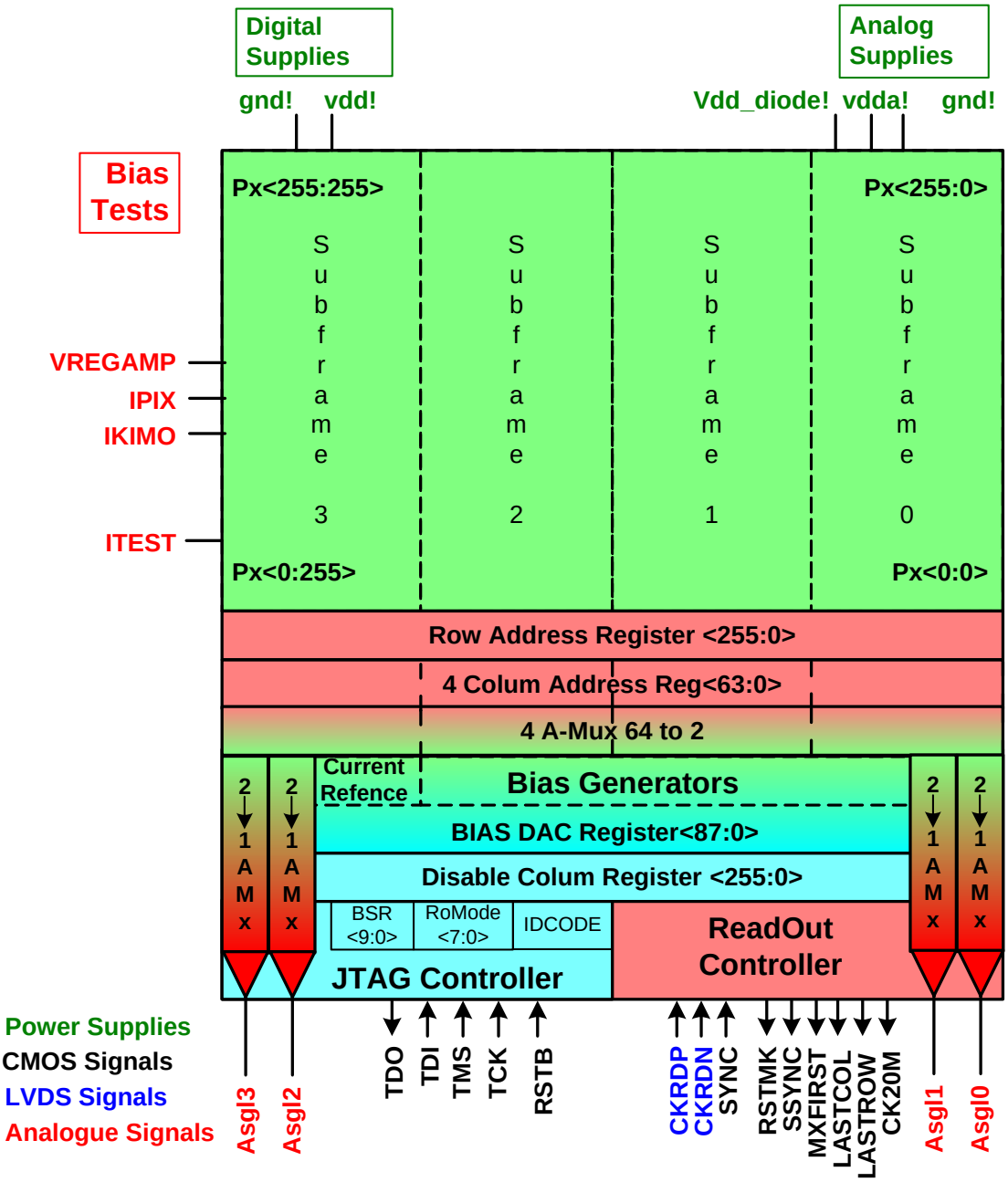
MimoStar chip family		
Version	Date	Description
MimoTEL	Submitted June 06	AMS 035 Opto Version, 256 x 256 pixels, Parallel outputs
3L	Submitted June 06	AMS 035 Opto Version, 640 x 320 pixels, Serial outputs
2	Submitted:June 05	AMS 035 Opto Version, 128 x 128 pixels
1	Submitted July 04	TSMC 025 Version

1 Introduction

MimoTEL, the third version of the MimoStar family, has been designed in C35B4O1, the AMS 0.35 µm opto process. Like MimoStar 1 and 2, it is a Monolithic Active Pixel Sensor prototype dedicated to vertex particle tracking in the EUDET telescope. The matrix is composed by 256 x 256 pixels of 30 µm pitch and based on self biased diode architectures. It is organised in 4 matrices, or subframes, of 256 lines x 64 columns, accessed in parallel during the readout. The individual pixel architecture, should meet the radiation tolerance and the low leakage current requirements.

The addressing of each subframe is sequential and starts from the upper left pixel up to the lower right pixel. The beginning of each subframe row is stamped by 2 dummy pixels acting as makers and having programmable levels.

Each subframe has its own analogue serial output, a single ended voltage output buffer running up to 20 MHz which gives a readout time of 850µs/frame.



MimoTEL functional view

Does not correspond to the floorplan; neither for the core, neither for the pad ring

MimoTEL is very simple to operate:

- Power On Reset or Reset on the RSTB pad
- Setup of the chip
  It is performed with programmable registers accessed via an embedded slow control interface. It consists to:
  - Load the DACs which bias the analogue blocks
  - If necessary, load the ReadOut Register with a specific configuration. The default setup on power on reset allows a normal readout once the biases have been set.
- Readout of the chip
  - The readout starts when the input "SYNC" token has its falling signal sampled by the LVDS readout input clock CKRD . It happens at the first rising edge of the 20MHz clock which follows the SYNC falling edge.
  - After a latency of 4 input clock cycles, the analogue signals appear on the output buffers
  - Digital maker outputs are available for the control of the readout process
  - Pixels are sequentially read out in a specific order explained later in the document
  - Successive pixel frames are read until the readout clock is stopped

A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

2 Control Interface

The control interface complies with the Boundary Scan, JTAG, IEEE 1149.1 Rev 1999 standard. It allows the access to the internal registers of the chip like the bias register and the readout mode selection register.
On Power-On-Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

2.1 *JTAG Instruction Set*

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	**5 Bit Code$_{16}$**	**Selected Register**	**Notes**
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG optional instruction
INTEST	03	BSR	JTAG optional instruction
CLAMP	04	BYPASS	JTAG optional instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
ID_CODE	0E	ID register	JTAG optional instruction
BIAS_GEN	0F	BIAS register	User instruction
DIS_COL	10	Disable Columns	User instruction
NU1	11		Reserved, Not Used
NU2	12		Reserved, Not Used
NU3	13		Reserved, Not Used
NU4	14		Reserved, Not Used
NU5	15		Reserved, Not Used
NU6	16		Reserved, Not Used
NU7	17		Reserved, Not Used
NU8	18		Reserved, Not Used
NU9	19		Reserved, Not Used
NU10	1A		Reserved, Not Used
NU11	1B		Reserved, Not Used
NU12	1C		Reserved, Not Used
RO_MODE1	1D	Read Out Mode1	User instruction
RO_MODE0	1E	Read Out Mode0	User instruction
BYPASS	1F	BYPASS	JTAG mandatory instruction

2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
BYPASS	1	R Only	
BSR	9	R/W	
ID_CODE	32	R Only	Fixed pattern
BIAS_GEN (11 DACs)	88	R/W	Previous value shifted out during write
DIS_COL	256	R/W	Previous value shifted out during write
RO_MODE1	8	R/W	Previous value shifted out during write
RO_MODE0	8	R/W	Previous value shifted out during write
NU1, …, NU12	0		Not implemented. For future use

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.2.2 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.3 Boundary Scan Register

The Boundary Scan Register, according with the JTAG instructions, tests and set the IO pads. The BSR is 9 bits long and allows the test of the following input and output pads

Bit #	Corresponding Pad	Type	Signal	Notes
8	LVDS CkRdP/CkRdN	Input	CkRd	Resulting CMOS signal after LVDS Receiver
7	ASync	Input	Sync	
6	SSync	Output	SSync	
5	Ck5M	Output	Ck5M	Internal only, Not used
4	Ck20M	Output	Ck20M	
3	RstMk	Output	RstMk	
2	LastRow	Output	LastRow	
1	LastCol	Output	LastCol	
0	MxFirst	Output	MxFirst	

2.2.4 ID_CODE Register

The Device Identification register is implemented is this third version. It is 32 bits long and has fixed value hardwired into the chip. When selected by the ID_CODE instruction or after the fixed value is shifted via TDO, the JTAG serial output of the chip.

ID_CODE register value is **0xFFFF8001**

2.2.5 RO_Mode Register0

The RO_Mode registers are 8 bits large; they allow the user to select specific features of the chip.
MimoTEL use only the RO_Mode Register0.

Bit #	Bit Name	Purpose	Default value	
7	Not Used			
6	Not Used			
5	DisLVDS	Disable LVDS, readout clock is not active anymore.	0	LVDS selected
4	SelMux	On MxFirst output pad, select the MuxFirst signal or the First_Pixel_of the Frame signal	1	MuxFirst Signal, active See § 3.4 Readout
3	EnaGain3	Select gain 3 for the serial differential output buffer	0	Gain 5
2	Not used		-	
1	Not Used			
0	EnaTstCol	Test Mode: Select the 2 Test Levels, IVTEST1 and IVTEST0, which emulate a pixel output	0	Normal mode

2.2.6 DIS_COL Register

The DIS_COL register is 256 bit wide. The purpose of this register is to disable the column current sources if a short circuit is suspected on a specific column. During the readout, even if a current source is disabled the corresponding column is selected, i.e. no columns are skipped. Obviously, the signal of the corresponding pixel has no signification.
The default value of the DIS_COL register is 0; it means that all current sources can be activated by the readout logic. Setting a bit to 1 disables the corresponding current source. The column <256> is on the left hand side while column<0> is on the right hand side. The organisation of the chip in 4 subframes of 64 columns has no matter to do with the DIS_COL register.

255 (Msb)	**0 (Lsb)**
DisCol<255>	**DisCol<0>**

2.2.7 BIAS_DAC Register

The BIAS_DAC register is 88 bits large; it sets simultaneously the 11 DAC registers.
As show bellow these 8-bit DACs set voltage and current biases.
After reset, the register is set to 0, a value which fixes the minimum power consumption of the circuit.
The current values of the DACs are read while the new values are downloaded during the access to the register.
The image of the value of some critical biases can be measured on corresponding test pads.

Bit range	DAC #	DAC Internal Name	DAC purpose	Corresponding Test Pad
87- 80	DAC10	IKIMO	External circuit monitoring	IKIMO
79- 72	DAC9	I4PIX	Pixel source follower bias. DAC with positive slope (0 to 255 µA; 1 µA step)	IPIX
71- 64	DAC8	V4TEST1	Test Level, emulates a pixel output. DAC with positive slope (0 to 2.55V; 10 mV step)	No pad
63- 56	DAC7	V4TEST0	Idem	No pad
55- 48	DAC6	V4REG3	Regulator voltage bias for the column amplifier (Gain 3 &5). DAC with negative slope ((3.3 to 0.75 V by step of 10 mV)	VREGAMP
47- 40	DAC5	V4REG2	Idem	No pad
39- 32	DAC4	V4REG1	Idem	No pad
31- 24	DAC3	V4REG0	Idem	No pad
23- 16	DAC2	I4REGAMP	Regulator current bias for column amplifier (G = 3 & 5) This DAC value is not very sensitive for test. DAC with positive slope (0 to 255 µA; 1 µA step)	No pad
15- 8	DAC1	I4AMP	Bias of column amplifier. DAC with positive slope (0 to 255 µA; 1 µA step)	No pad
7- 0	DAC0	ISLOWBUFSE	Bias of the single ended Output Buffers. DAC with positive slope (0 to 255 µA; 1 µA step)	No pad

3 Running MimoTEL

The following steps describe how to operate the ASIC.

3.1 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_COL is set to 0, i.e. all columns are selected
- RO_Mode is set to 0
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded.
The same has to be done for the RO_MODE0 and DIS_COL registers if the running conditions differ from defaults.
Finally the readout can be performed either in normal mode or in test mode.

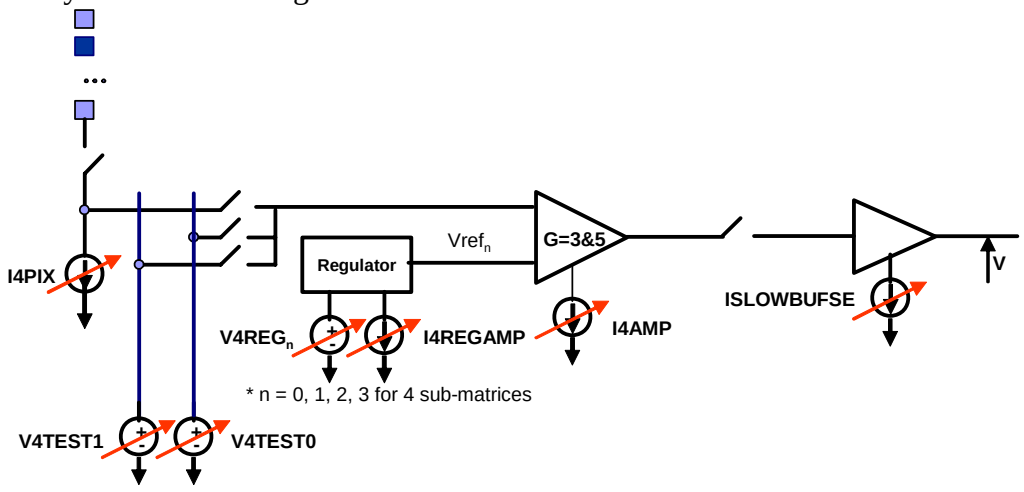
3.2 Biasing MimoTEL

The BIAS_DAC register has to be loaded before operating the chip.
The 11 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	Simulation			Resolution	Range	Experimental(1)
	$Code_{16}$ - $Code_{10}$	DacInternal current-µA	Output value			$Code_{16}$ –$Code_{10}$
IKIMO	64-100	100	1 V	10 mV	From 0 up to 2.55 V	0-0
I4PIX	1E-30	30	30 µA	1 µA	From 0 up to 255 µA	1-1
V4TEST1	C3–195	195	1.95 V	10 mV	From 0 up to 2.55 V	FA-250
V4TEST0	B9–185	185	1.85 V	10 mV	From 0 up to 2.55 V	E6-230
V4REG 3	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	**80-128**
V4REG 2	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	**80-128**
V4REG 1	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	**80-128**
V4REG 0	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	**80-128**
I4REG1	21–33	33	33 µA	1 µA	From 0 up to 255 µA	1-1
I4AMP	64–100	100	100 µA	1 µA	From 0 up to 255 µA	3-3
ISLOWBUFSE	64–100	100	100 µA	1 µA	From 0 up to 255 µA	A-10

Note 1: The HRES ploysilicon, used in the bias block, is missing for this submission. Experimental values correspond to the recalculated parameters that allow nevertheless the chip be operated. A new submission of the chip is in progress.

Bias synthetic block diagram



Note1: Vrefn ~= V4REGn – 1V

3.3 Setting the Readout_Mode Register

If the desired operating mode does not correspond to the default one, set the Readout_Mode0 register following the §2.2.5 information.

3.4 Readout

3.4.1 Signal protocol

Ones JTAG registers have been loaded, the readout of MimoTEL may initiate with the following signal protocol:

- The readout clock CKRD is started. This allows the output pad CK20M to generate a 20 MHz clock. This clock follows the input.
- The SYNC signal is set.
- The readout starts at the first rising edge of CKRD after SYNC signal disappears.
- Signal markers allow the monitoring of the readout and the analogue data sampling:
    - RstMk maker confirms that the internal reset of the readout logic is done.
    - SSync marker shows that the readout starts.
    - 4 extra CKRD clock cycles, after SYNC sampling, are necessary before the analogue signal of the first pixel appears on the output pad.
    - The MxFirst digital signal helps for a better sampling of the analogue output signals. The way it acts is set by the RO_Mode[4] bit.
        - RO_Mode[4] = 0: MxFirst is active during the duration of the first maker of the frame
        - RO_Mode[4] = 1: MxFirst is active on each pixel change on the analogue output i.e. it is a 20 MHz periodic signal.
    - LastCol is active when the last column of the current row is selected
    - LastRow is active when the last row of the frame is selected
    - Ck20M output shows the internal clock running as long as input clock is running.

3.4.2 Successive frames and resynchronisation

Successive pixel frames are read until the readout clock is stopped. A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

3.5 Analogue Data Format

Two types of signal can be generated

- Normal pixel signal
- Test signal.

3.5.1 Normal mode data format

In order to improve the readout speed MimoTEL is organized 4 subframes. Each subframe has its own analogue serial output, a single ended voltage output buffer running up to 20 MHz.
During the readout, the 4 subframes are accessed in parallel. For each subframe the addressing is done row by row, each pixel is accessed sequentially from the left side to right side. Each row contains 2 makers (acting as dummy pixels), and 64 active pixels. One can use the adjustable level of the 2 makers as a pattern recogniser. If the pixel coordinate format is specified as Px<Line, Column>, then for each subframe, the upper left pixel is Px<255, 63> while the lower right is Px<0, 0> and the makers of each beginning row are named Mk1 and Mk0. Thus the 4 parallel outputs generate respectively the following stream formats:

3.5.1.1 Format of the analogue ouput Asgl<3>

```
Mk1, Mk0, Px<255,255>, Px<255,254>,. . ., Px<255,192>
Mk1, Mk0, Px<254,255>,.Px<254,254>,. . ., Px<254,192>
. . . . . . . . . . . . . . . . . . . . . . . . . . . .
Mk1, Mk0, Px<  1,255>,.Px<  1,254>,. . ., Px<  1,192>
Mk1, Mk0, Px<  0,255>,.Px<  0,254>,. . ., Px<  0,192>
```

3.5.1.2 Format of the analogue ouput Asgl<2>

```
Mk1, Mk0, Px<255,191>, Px<255,190>,. . ., Px<255,128>
Mk1, Mk0, Px<254,191>,.Px<254,190>,. . ., Px<254,128>
. . . . . . . . . . . . . . . . . . . . . . . . . . . .
Mk1, Mk0, Px<  1,191>,.Px<  1,191>,. . ., Px<  1,128>
Mk1, Mk0, Px<  0,191>,.Px<  0,191>,. . ., Px<  0,128>
```

3.5.1.3 Format of the analogue ouput Asgl<1>

```
Mk1, Mk0, Px<255,127>, Px<255,126>,. . ., Px<255, 64>
Mk1, Mk0, Px<254,127>,.Px<254,126>,. . ., Px<254, 64>
. . . . . . . . . . . . . . . . . . . . . . . . . . . .
Mk1, Mk0, Px<  1,127>,.Px<  1,126>,. . ., Px<  1, 64>
Mk1, Mk0, Px<  0,127>,.Px<  0,126>,. . ., Px<  0, 64>
```

3.5.1.4 Format of the analogue ouput Asgl<0>

```
Mk1, Mk0, Px<255, 63>, Px<255, 62>,. . ., Px<255,  0>
Mk1, Mk0, Px<254, 63>,.Px<254, 62>,. . ., Px<254,  0>
. . . . . . . . . . . . . . . . . . . . . . . . . . . .
Mk1, Mk0, Px<  1, 63>,.Px<  1, 62>,. . ., Px<  1,  0>
Mk1, Mk0, Px<  0, 63>,.Px<  0, 62>,. . ., Px<  0,  0>
```

3.5.2 Test mode data format

During the test mode the pixel matrix is not anymore connected to the multiplexing electronic. In place of it, two test levels V4TEST1 (V1), V4TEST0 (V0) are available. They emulate two pixel level outputs. Actually these levels correspond to those of Marker 1 and Marker 0. They are adjustable via 2 DACs. Even and odd columns are alternatively connected to one of them. This pattern allows seeing the output signal changing and emulates the readout shift from one column of pixel to the other column of pixel.
Thus the 4 parallel outputs generate respectively the following stream formats:

Subframe 3, analogue ouput Asgl<3>: **V1, V0, V0, V1**, V1, V0, V0, V1 . . .
Subframe 2, analogue ouput Asgl<2>: **V0, V1, V1, V0**, V0, V1, V1, V0 . . .
Subframe 1, analogue ouput Asgl<1>: **V1, V0, V0, V1**, V1, V0, V0, V1 . . .
Subframe 0, analogue ouput Asgl<0>: **V0, V1, V1, V0**, V0, V1, V1, V0 . . .

3.6 MimoTEL Chronogram

The following chronograms describe typical access to the chip; Reset, JTAG download sequence and then the readout. This one starts with the initialisation phase followed by the successive row readouts as showed in the zoom.

3.6.1 Normal Readout

Figure 1 show the beginning of a typical normal data readout mode. After Reset and JTAG settings, one can see the initialisation phase of the readout of the first pixel row. The LastCol signal is active meanwhile the last pixel of a row is read. The last row of the frame makes the LastRow signal to be active. One of the 4 parallel analogue outputs is showed. One can distinguish the 2 makers placed at the beginning of each row.
Figure 2 is the zoom of the readout of the first row.
Figure 3 is an enlargement of the transition from one row to the successive one.
Figure 4 show the alternate option of the MxFirst signal. It is active only during the time the first maker appears i.e. just before the first pixel of the frame. This option is set via the RoMode register.

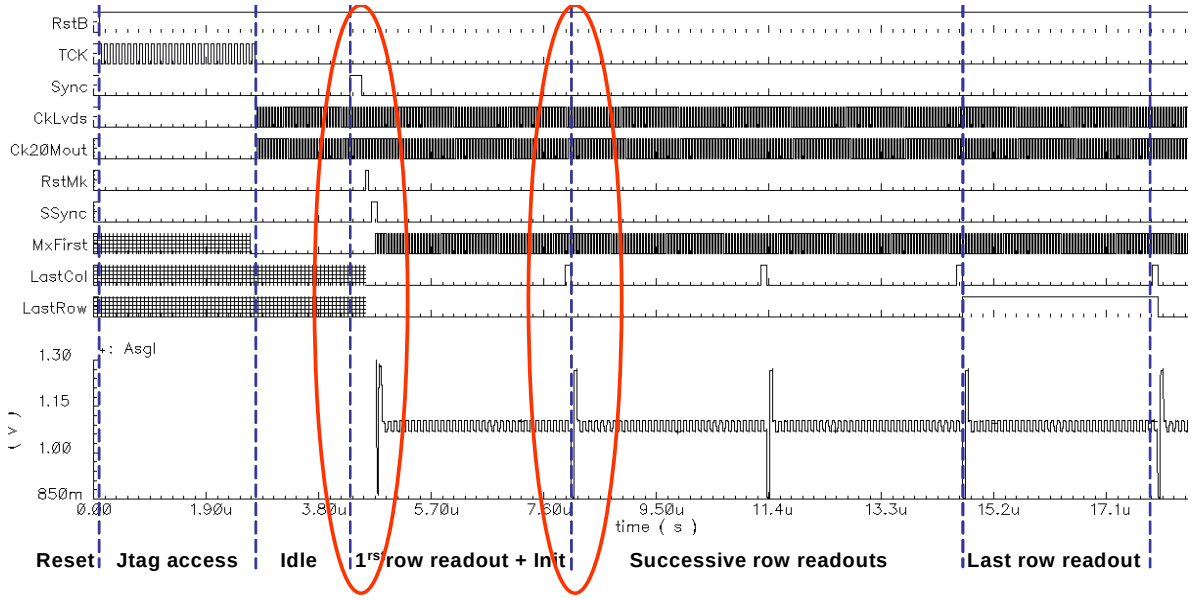


Figure 1

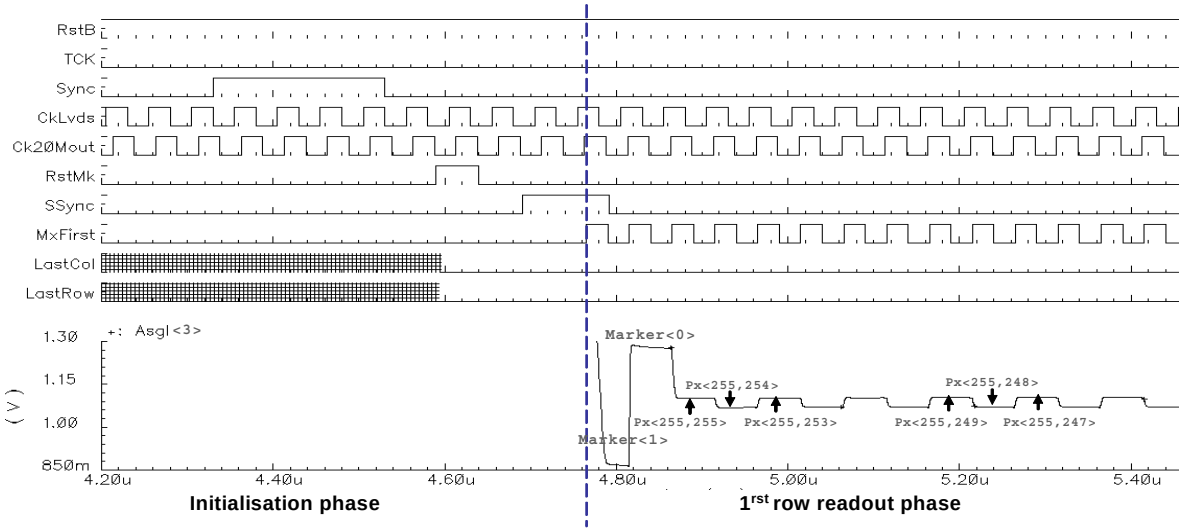


Figure 2

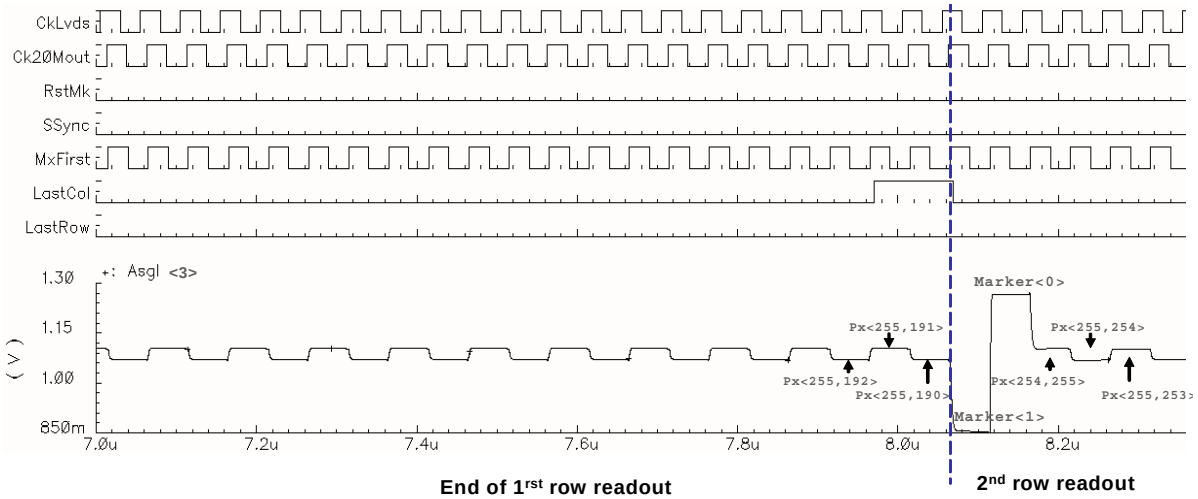


Figure 3

3.6.1.1 Alternate Mxfirst signal for normal readout

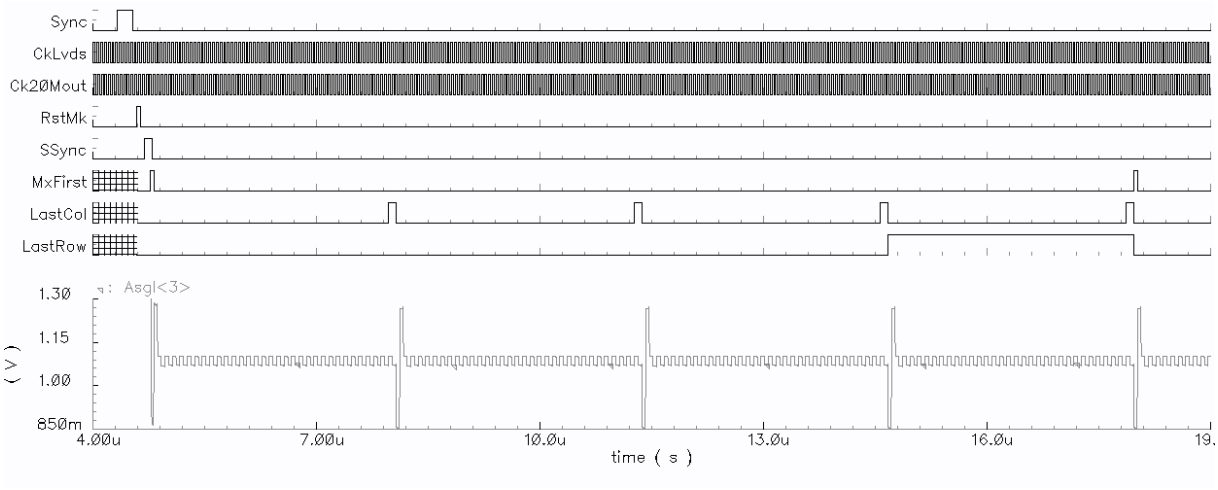
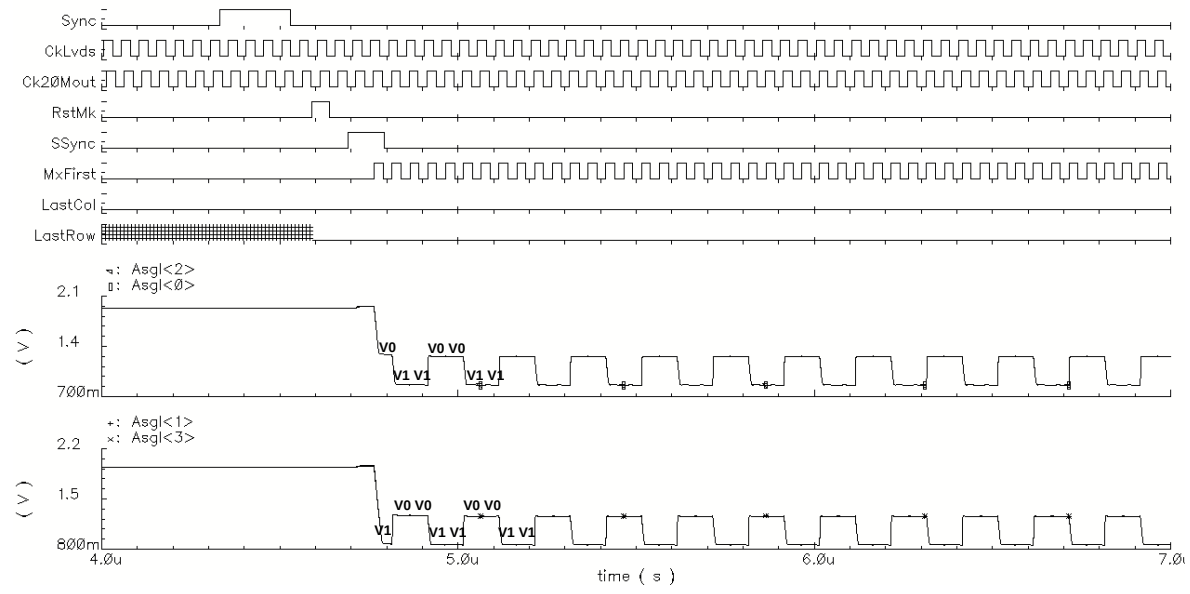


Figure 4

3.6.2 Test mode readout

The initialisation phase if the test mode is the same than in the normal mode. But it has to be noticed than the LastCol and LastRow makers are unavailable because the test mode has nothing to deal with the matrix and its line and column addressing registers. For the same reason the MxFirst maker is unavailable in the “First Pixel of frame mode” but only continuous mode.



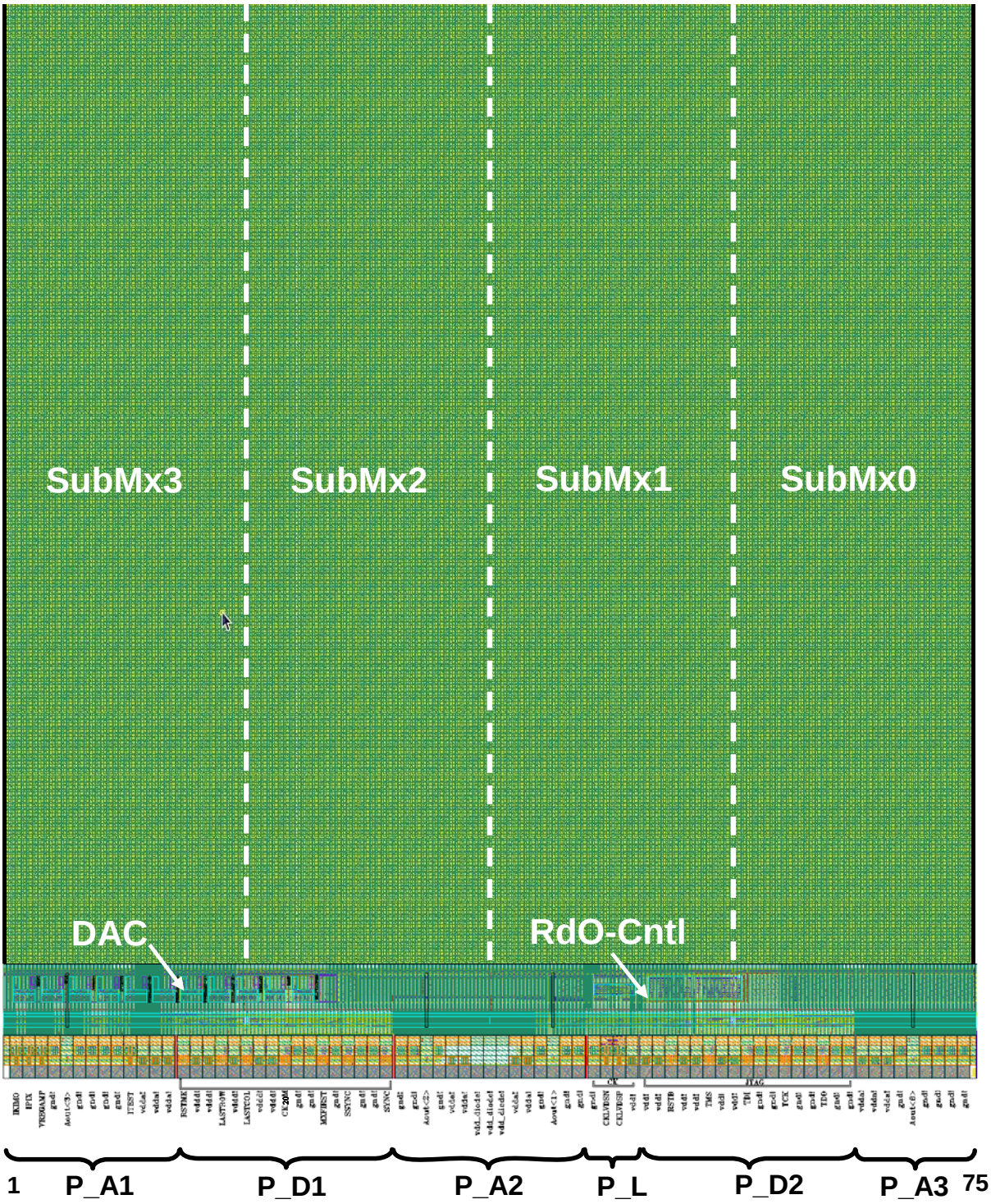
4 Pad Ring

The pad ring of the chip is build with

- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 6 functional independent parts. Each part has its own supply pads.

4.1 MimoTEL Pad Ring and Floor Plan View



Foundry submission information
MimoTEL has been designed in AMS C35B4O1 CMOS 0.35 µm.
The Process Design Kit V3.70 has been provided by CMP
CAD tools are CADENCE DFII 5.0 with DIVA and ASSURA rules

4.2 Pad List

Pad ring segment 1 – P_A1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
1	IKIMO	Analog I/O pad, 0 Ω serial	APRIOP	Gen Purpose DAC Output
2	IPIX	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
3	VREGAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Out, Test Purpose Only
4	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
5	Aout<3>	Direct Pad, no protections	DIRECTPAD	Analogue data out
6	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
7	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
8	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
9	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
10	ITEST	Analog I/O pad, 0 Ω serial	APRIOP	Internal Current Ref Source
11	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
12	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
13	vdda	Analogue Pad Supply	AVDDALLP	3.3 V

Pad ring segment – P_D1				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
14	RSTMK	Tri-State Output Buffer, 2 mA	BT2P	Readout Reset Marker
15	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
16	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
17	LastRow	Tri-State Output Buffer, 2 mA	BT2P	Last Row Maker
18	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
19	LastCol	Tri-State Output Buffer, 2 mA	BT2P	Last Column Marker
20	vddd	Pad supplying the output buffers	VDD3OP	3.3 V
21	vddd	Pad supplying the output buffers	VDD3OP	3.3 V
22	CK20M	Tri-State Output Buffer, 2 mA	BT2P	20 MHz Clock Out
23	gnd	Pad supplying the output buffers	GND3OP	Ground
24	gnd	Pad supplying the output buffers	GND3OP	Ground
25	MxFirst	Tri-State Output Buffer, 2 mA	BT2P	First pixel maker
26	gnd	Core logic and periphery cells supply	GND3RP	Ground periphery cells only
27	Ssync	Tri-State Output Buffer, 2 mA	BT2P	Readout Synchro. Start Marker
28	gnd	Core logic and periphery cells supply	GND3RP	Ground periphery cells only
29	gnd	Core logic and periphery cells supply	GND3RP	Ground periphery cells only
30	Sync	CMOS Input Buffer	ICP	Readout Input token

Pad ring segment – P_A2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
31	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
32	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
33	Aout<2>	Direct Pad, no protections	DIRECTPAD	Analogue data out
34	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
35	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
36	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
37	vdd_diode	Direct pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
38	vdd_diode	Direct pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
39	vdd_diode	Direct pad, no protections	DIRECTPAD	Pixel Diode Bias, 3.3V
40	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
41	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
42	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
43	Aout<1>	Direct Pad, no protections	DIRECTPAD	Analogue data out

44	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core
45	gnd	Core logic and periphery cells supply	AGNDALLP	Ground periphery & core

Pad ring segment 3 – P_L				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
46	gnd	LVDS Pad Ground	AGNDALLP	Ground for LVDS Pad
47	CKRN	LVDS In -	Full Custom	Readout Clock Signal
48	CKRP	LVDS In +		
49	vdd	LVDS Pad Supply	AVDDALLP	3.3V for LVDS Pad

Pad ring segment 2 – P_D2				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
50	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
51	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
52	RSTB	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Asynchronous Active Low Reset
53	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
54	vddd	Core logic and periphery cells supply	VDD3RP	3.3 V
55	TMS	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
56	vddd	Pad supplying the output buffers	VDD3OP	3.3 V
57	vddd	Pad supplying the output buffers	VDD3OP	3.3 V
58	TDI	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
59	gnd	Pad supplying the output buffers	GND3OP	Ground
60	gnd	Pad supplying the output buffers	GND3OP	Ground
61	TCK	CMOS Clock Input Buffer, 2 mA	ICCK2P	JTAG Clock
62	gnd	Core logic and periphery cells supply	GND3RP	Ground
63	gnd	Core logic and periphery cells supply	GND3RP	Ground
64	TDO	Tri-State Output Buffer, 4 mA	BT4P	JTAG Serial Data Out
65	gnd	Core logic and periphery cells supply	GND3RP	Ground
66	gnd	Core logic and periphery cells supply	GND3RP	Ground

Pad ring segment – P_A3				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
67	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
68	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
69	vdda	Analogue Pad Supply	AVDDALLP	3.3 V
70	gnd	Core logic and periphery cells supply	AGNDALLP	Ground
71	Aout<0>	Direct Pad, no protections	DIRECTPAD	Analogue data out
72	gnd	Core logic and periphery cells supply	AGNDALLP	Ground
73	gnd	Core logic and periphery cells supply	AGNDALLP	Ground
74	gnd	Core logic and periphery cells supply	AGNDALLP	Ground
75	gnd	Core logic and periphery cells supply	AGNDALLP	Ground