MimoStar3
User Manual

MimoStar2 User Manual

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# Document history

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>March 2007</td>
<td>Based on MimoStar2 Version</td>
</tr>
</tbody>
</table>

# MimoStar chip

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
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<tbody>
<tr>
<td>3</td>
<td>Submitted June 06</td>
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</tr>
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<td>AMS 035 Opto Version, 128 x 128 pixels</td>
</tr>
<tr>
<td>1</td>
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<td>TSMC 025 Version</td>
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</tbody>
</table>
1 Introduction ................................................................................................................. 3
2 Control Interface ............................................................................................................ 4
  2.1 JTAG Instruction Set .............................................................................................. 4
  2.2 JTAG Register Set ................................................................................................. 5
    2.2.1 Instruction Register ........................................................................................ 5
    2.2.2 Bypass Register ............................................................................................ 5
    2.2.3 Boundary Scan Register .............................................................................. 5
    2.2.4 ID_CODE Register ..................................................................................... 5
    2.2.5 DIS_COL Register ...................................................................................... 6
    2.2.6 RO_Mode Register0 ................................................................................... 6
    2.2.7 BIAS_DAC Register ................................................................................... 6
3 Running MimoStar3 ...................................................................................................... 7
  3.1 After reset ............................................................................................................. 7
  3.2 Biasing MimoStar3 ............................................................................................... 7
  3.3 Setting the Readout_Mode Register ...................................................................... 8
  3.4 Readout ................................................................................................................. 8
    3.4.1 Signal protocol ............................................................................................ 8
    3.4.2 Successive frames and resynchronisation ................................................... 8
  3.5 Analogue Data Format .......................................................................................... 8
    3.5.1 Normal mode data format ........................................................................... 9
    3.5.2 Test mode data format ................................................................................ 9
  3.6 MimoStar3 Chronograms .................................................................................... 10
    3.6.1 Normal Readout ........................................................................................ 10
      3.6.1.1 Readout synchronisation .................................................................... 10
    3.6.2 Test mode readout ..................................................................................... 12
    3.6.3 Main Signal Specifications ........................................................................... 13
  3.7 ADC .................................................................................................................... 13
    3.7.1 ADC_SEL register ....................................................................................... 13
4 Pad Ring ..................................................................................................................... 15
  4.1 MimoStar3 Pad Ring and Floor Plan View ........................................................... 15
  4.2 Pad List ............................................................................................................... 15
1 Introduction

Mimostar3, the third version of the MimoStar family, has been designed in C35B4O1, the AMS 0.35 µm opto process. Like MimoStar 1 and 2, it is a Monolithic Active Pixel Sensor prototype dedicated to vertex particle tracking in a future update of the STAR vertex detector. The matrix is composed by 320 x 640 pixels of 30 µm pitch and based on self biased diode architectures. It is organised in 10 matrices, or subframes, of 320 lines x 64 columns, accessed in parallel during the readout. The individual pixel architecture, should meet the radiation tolerance and the low leakage current requirements. Actually Mimostar3 prototype has the half size of the final circuit which is foreseen with 640 lines.

The addressing of each subframe is sequential and starts from the upper left pixel up to the lower right pixel. The beginning of each subframe row is stamped by 2 pixels acting as makers and having programmable levels. The 10 subframes are gathered in 2 banks. Each bank has its own analogue serial output, a differential current output buffer running up to 50 MHz allowing a readout time of 2 ms/frame.

MimoStar3 is very simple to operate:
- Power On Reset or Reset on RSTB pad
- Setup of the chip
  It is performed with programmable registers accessed via an embedded slow control interface. It consists to:
  - Load the DACs which bias the analogue blocks

March 2007  MimoStar3 User Manual 3
• If necessary, load the ReadOut Register with a specific configuration. The default setup on power on reset allows a normal readout once the biases have been set.
• Readout of the chip
  • The chip is driven by a 50 MHz clock. The readout starts when the input "SYNC" token has its falling signal sampled by the internal 5 MHz clock. It happens at the first falling edge of the internal clock which follows the SYNC falling edge.
  • Readout synchronisation is achieved by the digital marker MxFirst which becomes active when the analogue signal of the first pixel appears
  • Other digital markers are available for the control of the readout process
  • Pixels are sequentially read out in a specific order explained later in the document
  • Successive pixel frames are read until the readout clock is stopped

A frame resynchronisation can be performed at any time by setting up the "SYNC” token again.

In addition some test features have been implemented in this version:
• 2 single-ended voltage output buffers, one per bank, allows a simpler readout at low frequency. The purpose is to verify coarse parameters, like analogue baseline, directly on the wafer with a probe card.
• An 8 bit ADC running at 100 kHz/word allows some parameter measurements like voltage supplies and current consumption.
• An embedded temperature probe provides its analogue output via 2 output pads.

2 Control Interface

The control interface of MimoStar3 complies with the Boundary Scan, JTAG, IEEE 1149.1 Rev 1999 standard. It allows the access to the internal registers of the chip like the bias register and the readout mode selection register.

On Power-On-Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

2.1 JTAG Instruction Set

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>5 Bit Code_{16}</th>
<th>Selected Register</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST</td>
<td>01</td>
<td>BSR</td>
<td>JTAG mandatory instruction</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>02</td>
<td>BYPASS</td>
<td>JTAG mandatory instruction</td>
</tr>
<tr>
<td>INTEST</td>
<td>03</td>
<td>BSR</td>
<td>JTAG optional instruction</td>
</tr>
<tr>
<td>CLAMP</td>
<td>04</td>
<td>BYPASS</td>
<td>JTAG optional instruction</td>
</tr>
<tr>
<td>SAMPLE_PRELOAD</td>
<td>05</td>
<td>BSR</td>
<td>JTAG mandatory instruction</td>
</tr>
<tr>
<td>ID_CODE</td>
<td>0E</td>
<td>ID register</td>
<td>JTAG optional instruction</td>
</tr>
<tr>
<td>BIAS_GEN</td>
<td>0F</td>
<td>BIAS register</td>
<td>User instruction</td>
</tr>
<tr>
<td>DIS_COL</td>
<td>10</td>
<td>Disable Columns</td>
<td>User instruction</td>
</tr>
<tr>
<td>ADC_SEL</td>
<td>11</td>
<td>AnalogIn Select reg</td>
<td>User instruction</td>
</tr>
<tr>
<td>ADC_ROR</td>
<td>12</td>
<td>ReadOut Register</td>
<td>User instruction</td>
</tr>
<tr>
<td>NU1</td>
<td>13</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU2</td>
<td>14</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU3</td>
<td>15</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU4</td>
<td>16</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU5</td>
<td>17</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU6</td>
<td>18</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU7</td>
<td>19</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU8</td>
<td>1A</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU9</td>
<td>1B</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>NU10</td>
<td>1C</td>
<td></td>
<td>Reserved, Not Used</td>
</tr>
<tr>
<td>RO_MODE1</td>
<td>1D</td>
<td>Read Out Mode1</td>
<td>User instruction</td>
</tr>
<tr>
<td>RO_MODE0</td>
<td>1E</td>
<td>Read Out Mode0</td>
<td>User instruction</td>
</tr>
<tr>
<td>BYPASS</td>
<td>1F</td>
<td>BYPASS</td>
<td>JTAG mandatory instruction</td>
</tr>
</tbody>
</table>
2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Size</th>
<th>Access</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>INSTRUCTION REG</td>
<td>5</td>
<td>R/W</td>
<td>Instruction Register</td>
</tr>
<tr>
<td>BYPASS</td>
<td>1</td>
<td>R Only</td>
<td></td>
</tr>
<tr>
<td>BSR</td>
<td>11</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>ID_CODE</td>
<td>32</td>
<td>R Only</td>
<td>Pattern fixed at 0xFFFF0001</td>
</tr>
<tr>
<td>BIAS_GEN (20 DACs)</td>
<td>160</td>
<td>R/W</td>
<td>Previous value shifted out during write</td>
</tr>
<tr>
<td>DIS_COL</td>
<td>640</td>
<td>R/W</td>
<td>Previous value shifted out during write</td>
</tr>
<tr>
<td>ADC_SEL</td>
<td>20</td>
<td>R/W</td>
<td>Previous value shifted out during write</td>
</tr>
<tr>
<td>ADC_ROR</td>
<td>11</td>
<td>R Only</td>
<td>Previous ADC value shifted</td>
</tr>
<tr>
<td>RO_MODE1</td>
<td>8</td>
<td>R/W</td>
<td>Previous value shifted out during write</td>
</tr>
<tr>
<td>RO_MODE0</td>
<td>8</td>
<td>R/W</td>
<td>Previous value shifted out during write</td>
</tr>
<tr>
<td>NU1, …, NU10</td>
<td>0</td>
<td></td>
<td>Not implemented. For future use</td>
</tr>
</tbody>
</table>

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of MimoStar2 is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

\[
\begin{array}{cccc}
X & X & X & 1 & 0
\end{array}
\]

2.2.2 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.3 Boundary Scan Register

The Boundary Scan Register, according with the JTAG instructions, tests and set the IO pads. The MimoStar3 BSR is 11 bits long and allows the test of the following input and output pads

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Corresponding Pad</th>
<th>Type</th>
<th>Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>LVDS CkRdP/CkRdN</td>
<td>Input</td>
<td>CkRd</td>
<td>Resulting CMOS signal after LVDS Receiver</td>
</tr>
<tr>
<td>9</td>
<td>ASync</td>
<td>Input</td>
<td>Sync</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CkADC</td>
<td>Input</td>
<td>CkADC</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>StartADC</td>
<td>Input</td>
<td>StarADC</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SSync</td>
<td>Output</td>
<td>SSync</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Ck5M</td>
<td>Output</td>
<td>Ck5M</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Ck10M</td>
<td>Output</td>
<td>Ck10M</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RstMk</td>
<td>Output</td>
<td>RstMk</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>LastRow</td>
<td>Output</td>
<td>LastRow</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>LastCol</td>
<td>Output</td>
<td>LastCol</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>MxFirst</td>
<td>Output</td>
<td>MxFirst</td>
<td></td>
</tr>
</tbody>
</table>

2.2.4 ID_CODE Register

The Device Identification register is implemented is this third version. It is 32 bits long and has fixed value hardwired into the chip. When selected by the ID_CODE instruction or after the fixed value is shifted via TDO, the JTAG serial output of the chip.

Mimostar3 ID_CODE register value is **0xFFFF0001**
2.2.5 DIS_COL Register

The DIS_COL register is 640 bit wide. The purpose of this register is to disable the column current sources if a short circuit is suspected on a specific column. During the readout, even if a current source is disabled the corresponding column is selected, i.e. no columns are skipped. Obviously, the signal of the corresponding pixel has no signification.

The default value of the DIS_COL register is 0; it means that all current sources can be activated by the readout logic. Setting a bit to 1 disables the corresponding current source. In MimoStar2, the column<639> is on the left hand side while column<0> is on the right hand side. The organisation of the chip in 10 subframes of 64 columns has no matter to do with the DIS_COL register.

<table>
<thead>
<tr>
<th>640 (Msb)</th>
<th>0 (Lsb)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DisCol&lt;639&gt;</td>
<td>DisCol&lt;0&gt;</td>
</tr>
</tbody>
</table>

2.2.6 RO_Mode Register0

The RO_Mode registers are 8 bits large; they allow the user to select specific features of the chip. MimoStar3 only use RO_Mode Register0.

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Bit Name</th>
<th>Purpose</th>
<th>Default value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SelJtagCk</td>
<td>Select TCK as the ADC clock in place of the external CkADC signal</td>
<td>0 Ext CkADC selected</td>
</tr>
<tr>
<td>6</td>
<td>SelFull</td>
<td>Set the row shift register to 640 in place of 320 bits. This option is designed to emulate a 640 x 640 pixel matrix.</td>
<td>0 Normal mode, 320 row shift register selected</td>
</tr>
<tr>
<td>5</td>
<td>DisLVDS</td>
<td>Disable LVDS, readout clock is not active anymore.</td>
<td>0 LVDS selected</td>
</tr>
<tr>
<td>4</td>
<td>SelMux</td>
<td>On MxFirst output, select MuxFirst signal or First Pixel of First Frame signal</td>
<td>1 MuxFirst Signal, active See § 3.4 Readout</td>
</tr>
<tr>
<td>3</td>
<td>EnaGain3</td>
<td>Select gain 3 for the serial differential output buffer</td>
<td>0 Gain 5</td>
</tr>
<tr>
<td>2</td>
<td>Not used</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>BufCopy</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>EnaTstCol</td>
<td>Test Mode: Select the 2 Test Levels, IVTEST1 and IVTEST0, which emulate a pixel output</td>
<td>0 Normal mode</td>
</tr>
</tbody>
</table>

2.2.7 BIAS_DAC Register

The BIAS_DAC register is 160 bits large; it sets simultaneously the 20 DAC registers. As show bellow these 8-bit DACs set voltage and current biases.

After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit.

The current values of the DACs are read while the new values are downloaded during the access to the register. The image of the value of some critical biases can be measured on corresponding test pads.

<table>
<thead>
<tr>
<th>Bit range</th>
<th>DAC #</th>
<th>DAC Internal Name</th>
<th>DAC purpose</th>
<th>Corresponding Test Pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>159-152</td>
<td>DAC19</td>
<td>IKIMO</td>
<td>External circuit monitoring</td>
<td>IKIMO</td>
</tr>
<tr>
<td>151-144</td>
<td>DAC18</td>
<td>I4PIX</td>
<td>Pixel source follower bias. DAC with positive slope (0 to 255 µA; 1 µA step)</td>
<td>IPIX</td>
</tr>
<tr>
<td>143-136</td>
<td>DAC17</td>
<td>V4TEST1</td>
<td>Test Level, emulates a pixel output. DAC with positive slope (0 to 2.55V; 10 mV step). Marker1</td>
<td>No pad</td>
</tr>
<tr>
<td>135-128</td>
<td>DAC16</td>
<td>V4TEST0</td>
<td>IDEM. Marker0</td>
<td>No pad</td>
</tr>
<tr>
<td>127-120</td>
<td>DAC15</td>
<td>V4REG9</td>
<td>Regulator voltage bias for the column amplifier (Gain 3 &amp;5). DAC with negative slope ((3.3 to 0.75 V by step of 10 mV)</td>
<td>No pad</td>
</tr>
<tr>
<td>119-112</td>
<td>DAC14</td>
<td>V4REG8</td>
<td>Idem</td>
<td>No pad</td>
</tr>
<tr>
<td>111-104</td>
<td>DAC13</td>
<td>V4REG7</td>
<td>Idem</td>
<td>No pad</td>
</tr>
<tr>
<td>103-96</td>
<td>DAC12</td>
<td>V4REG6</td>
<td>Idem</td>
<td>No pad</td>
</tr>
<tr>
<td>95-88</td>
<td>DAC11</td>
<td>V4REG5</td>
<td>Idem</td>
<td>No pad</td>
</tr>
</tbody>
</table>
Running MimoStar3

The following steps describe how to operate MimoStar3.

3.1 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_COL is set to 0, i.e. all columns are selected
- RO_Mode is set to 0
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded.

The same for the RO_MODE0 and DIS_COL registers if the running conditions differ from defaults. Finally the readout can be performed either in normal mode or in test mode.

3.2 Biasing MimoStar3

The BIAS_DAC register has to be loaded before operating MimoStar3.

The 20 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

<table>
<thead>
<tr>
<th>Internal DAC Name</th>
<th>Simulation</th>
<th>Resolution</th>
<th>Range</th>
<th>Experimental (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IKIMO</td>
<td>64-100</td>
<td>100</td>
<td>1 V</td>
<td>From 0 up to 2.55 V</td>
</tr>
<tr>
<td>I4PIX</td>
<td>1E-30</td>
<td>30</td>
<td>30 µA</td>
<td>From 0 up to 255 µA</td>
</tr>
<tr>
<td>V4TEST1</td>
<td>C3-195</td>
<td>195</td>
<td>1.95 V</td>
<td>From 0 up to 2.55 V</td>
</tr>
<tr>
<td>V4TEST0</td>
<td>B9-185</td>
<td>185</td>
<td>1.85 V</td>
<td>From 0 up to 2.55 V</td>
</tr>
<tr>
<td>V4REG 9-0</td>
<td>23-35</td>
<td>35</td>
<td>2.95 V</td>
<td>From 3.3 down to 0.75 V</td>
</tr>
<tr>
<td>I4REG1</td>
<td>21-33</td>
<td>33</td>
<td>33 µA</td>
<td>1 µA From 0 up to 255 µA</td>
</tr>
<tr>
<td>I4AMP</td>
<td>64-100</td>
<td>100</td>
<td>100 µA</td>
<td>From 0 up to 255 µA</td>
</tr>
<tr>
<td>I4INTBUF</td>
<td>64-100</td>
<td>100</td>
<td>100 µA</td>
<td>From 0 up to 255 µA</td>
</tr>
<tr>
<td>V4BUF1-0</td>
<td>5C-92</td>
<td>92</td>
<td>0.92 V</td>
<td>10 mV From 0 up to 2.55 V</td>
</tr>
<tr>
<td>I4BUF</td>
<td>28-40</td>
<td>40</td>
<td>40 µA</td>
<td>1 µA From 0 up to 255 µA</td>
</tr>
</tbody>
</table>

Note 1: The HRES polysilicon, used in the bias block, is missing for this submission. Experimental values correspond to the recalculated parameters that allow nevertheless the chip be operated. A new submission of the chip is in progress.
Bias synthetic block diagram

Note1: Vrefn \( \approx \) V4REGn – 1V

3.3 Setting the Readout_Mode Register
If the desired operating mode does not correspond to the default one, set the Readout_Mode register following the §2.2.6.

3.4 Readout

3.4.1 Signal protocol
Ones JTAG registers have been loaded, the readout of MimoStar3 may initiate with the following signal protocol:

- The readout clock is started. This allows the CK10M output pad to generate a 10 MHz clock. This clock follows the input clock with a 1/10 ratio if the 100 MHz is selected.
- The SYNC signal is set.
- The readout starts at the first rising edge of CK10M of after SYNC signal disappears.
- Signal markers allow the readout monitoring and the analogue data sampling:
  - RstMk maker confirms the internal reset of the readout logic.
  - SSync marker shows that the readout starts.
  - 4 extra CK10M clock cycles, after SYNC sampling, are necessary before the first pixel analogue signal appears on the selected output(s).
  - The MxFirst digital signal helps for a better sampling of the analogue output signals. The way it acts is set by the RO_Mode[4] bit.
    - RO_Mode[4] = 0: MxFirst is active only on the first pixel of the frame
    - RO_Mode[4] = 1: MxFirst is active on each pixel change on the parallel analogue output i.e. it is a10 MHz periodic signal.
      - Used with the 100 MHz serial mode (see serial data format bellow), its period shows when one pixel index has been read in all the subframes (2 real + 8 virtual).
  - LastCol is active when the last column of the current row is selected
  - LastRow is active when the last row of the frame is selected

3.4.2 Successive frames and resynchronisation
Successive pixel frames are read until the readout clock is stopped.
A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

3.5 Analogue Data Format
Two types of signal can be generated on the serial analogue outputs
- Normal pixel signal
- Test signal
### 3.5.1 Normal mode data format

In order to improve the readout speed Mimostar3 is organized in subframes, i.e. 10 subframes for this prototype. During the readout, the 10 subframes are accessed in parallel. For each subframe the addressing is done row by row, each pixel is accessed sequentially from the left side to right side. Each row contains 2 markers (acting as dummy pixels), and 64 active pixels. One can use the adjustable level of the 2 markers as a pattern recogniser. If the pixel coordinate format is specified as P<Line, Column>, then for each subframe, the upper left pixel is P<319, 63> while the lower right is P<0, 0> and the markers of each beginning row are named Mk1 and Mk0. The 10 subframes are themselves gathered in 2 banks. The two banks are readout in parallel; each one has its own analogue serial output. Thus in each bank, the readout consists to access successively one pixel of each of the 5 subframes and then turning back to the first subframe in order to read its next pixel.

For Mimostar3 the left hand side subframe is named Sf9 and the right hand side is Sf0. Thus the normal data stream format for the bank1 on the analogue output<1> is:

```
Sf9Mk1       ,Sf8Mk1       ,Sf7Mk1       ,Sf6Mk1       ,Sf5Mk1       ,
Sf9Mk0       ,Sf8Mk0       ,Sf7Mk0       ,Sf6Mk0       ,Sf5Mk0       ,
Sf9Px<319,63>,Sf8Px<319,63>,Sf7Px<319,63>,Sf6Px<319,63>,Sf5Px<319,63>,
Sf9Px<319,62>,Sf8Px<319,62>,Sf7Px<319,62>,Sf6Px<319,62>,Sf5Px<319,62>,
Sf9Px<319, 0>,Sf8Px<319, 0>,Sf7Px<319, 0>,Sf6Px<319, 0>,Sf5Px<319, 0>,
Sf9Mk1       ,Sf8Mk1       ,Sf7Mk1       ,Sf6Mk1       ,Sf5Mk1       ,
Sf9Mk0       ,Sf8Mk0       ,Sf7Mk0       ,Sf6Mk0       ,Sf5Mk0       ,
Sf9Px<318,63>,Sf8Px<318,63>,Sf7Px<318,63>,Sf6Px<318,63>,Sf5Px<318,63>,
Sf9Px<318,62>,Sf8Px<318,62>,Sf7Px<318,62>,Sf6Px<318,62>,Sf5Px<318,62>,
Sf9Px<318, 0>,Sf8Px<318, 0>,Sf7Px<318, 0>,Sf6Px<318, 0>,Sf5Px<318, 0>,
Sf9Mk1       ,Sf8Mk1       ,Sf7Mk1       ,Sf6Mk1       ,Sf5Mk1       ,
Sf9Mk0       ,Sf8Mk0       ,Sf7Mk0       ,Sf6Mk0       ,Sf5Mk0       ,
Sf9Px<  0,63>,Sf8Px<  0,63>,Sf7Px<  0,63>,Sf6Px<  0,63>,Sf5Px<  0,63>,
Sf9Px<  0,62>,Sf8Px<  0,62>,Sf7Px<  0,63>,Sf6Px<  0,62>,Sf5Px<  0,62>,
Sf9Px<  0, 0>,Sf8Px<  0, 0>,Sf7Px<  0, 0>,Sf6Px<  0, 0>,Sf5Px<  0, 0>,
```

For bank0 the format on the analogue output<0> is:

```
Sf4Mk1       ,Sf3Mk1       ,Sf2Mk1       ,Sf1Mk1       ,Sf0Mk1       ,
Sf4Mk0       ,Sf3Mk0       ,Sf2Mk0       ,Sf1Mk0       ,Sf0Mk0       ,
Sf4Px<319,63>,Sf3Px<319,63>,Sf2Px<319,63>,Sf1Px<319,63>,Sf0Px<319,63>,
Sf4Px<319,62>,Sf3Px<319,62>,Sf2Px<319,62>,Sf1Px<319,62>,Sf0Px<319,62>,
Sf4Px<319, 0>,Sf3Px<319, 0>,Sf2Px<319, 0>,Sf1Px<319, 0>,Sf0Px<319, 0>,
Sf4Mk1       ,Sf3Mk1       ,Sf2Mk1       ,Sf1Mk1       ,Sf0Mk1       ,
Sf4Mk0       ,Sf3Mk0       ,Sf2Mk0       ,Sf1Mk0       ,Sf0Mk0       ,
Sf4Px<318,63>,Sf3Px<318,63>,Sf2Px<318,63>,Sf1Px<318,63>,Sf0Px<318,63>,
Sf4Px<318,62>,Sf3Px<318,62>,Sf2Px<318,62>,Sf1Px<318,62>,Sf0Px<318,62>,
Sf4Px<318, 0>,Sf3Px<318, 0>,Sf2Px<318, 0>,Sf1Px<318, 0>,Sf0Px<318, 0>,
Sf4Mk1       ,Sf3Mk1       ,Sf2Mk1       ,Sf1Mk1       ,Sf0Mk1       ,
Sf4Mk0       ,Sf3Mk0       ,Sf2Mk0       ,Sf1Mk0       ,Sf0Mk0       ,
Sf4Px<  0,63>,Sf3Px<  0,63>,Sf2Px<  0,63>,Sf1Px<  0,63>,Sf0Px<  0,63>,
Sf4Px<  0,62>,Sf3Px<  0,62>,Sf2Px<  0,62>,Sf1Px<  0,62>,Sf0Px<  0,62>,
Sf4Px<  0, 0>,Sf3Px<  0, 0>,Sf2Px<  0, 0>,Sf1Px<  0, 0>,Sf0Px<  0, 0>,
```

### 3.5.2 Test mode data format

During the test mode the pixel matrix is not connected to the multiplexing electronic. In place of it, two test levels V4TEST1 (V1), V4TEST0 (V0) are available. They emulate the readout shift from one column of pixel to the other column of pixel. Actually these levels correspond to those of Marker 1 and Marker 0. They are adjustable via 2 DACs. Even and odd columns amplifiers are alternatively connected to one of them. The V1 and V0 levels are connected to the multiplexing electronic with a specific pattern. This pattern allows seeing the output signal changing. Thus the test data stream has the following format:

```
For Mimostar3 the left hand side subframe is named Sf9 and the right hand side is Sf0. Thus the normal data stream format for the bank1 on the analogue output<1> is:
```
Analogue output <1> format:
Sf9V1, Sf8V0, Sf7V1, Sf6V0, Sf5V1, Sf9V0, Sf8V1, Sf7V0, Sf6V1, Sf5V0,
Sf9V0, Sf8V1, Sf7V0, Sf6V1, Sf5V0, Sf9V1, Sf8V0, Sf7V1, Sf6V0, Sf5V1,

Analogue output <0> format:
Sf4V0, Sf3V1, Sf2V0, Sf1V1, Sf0V0, Sf4V1, Sf3V0, Sf2V1, Sf1V0, Sf0V1
Sf4V1, Sf3V0, Sf2V1, Sf1V0, Sf0V1, Sf4V0, Sf3V1, Sf2V0, Sf1V1, Sf0V0

3.6 MimoStar3 Chronograms

The following chronograms describe typical access to the chip; Reset, JTAG download sequence and then the
readout. This one starts with the initialisation phase followed by the successive row readouts as showed in the
zoom.

3.6.1 Normal Readout

Figure 1 show the beginning of a typical normal data readout mode. After Reset and JTAG settings, one can see
the initialisation phase of the readout of the first pixel row. The LastCol signal is active meanwhile the last pixel
of a row is read. The last row of the frame makes the LastRow signal to be active. The 2 serial analogue outputs
are showed. One can distinguish the 2 markers placed at the beginning of each row.

3.6.1.1 Readout synchronisation

The simplest way to get a readout synchronisation on the analogue data is to use the MxFirst signal in
“First_Pixel_of_Frame” mode which becomes active when the first pixel is ready on the analogue output. It
makes the data acquisition independent of the latency which exists between the start of the readout (Sync) and
the appearance of the data.

Nevertheless if it is impossible for the user to use MxFirst, the synchronisation on the analogue data is possible
by counting the number of the CK10M cycles. The latency between the Sync signal falling edge and the rising
edge of the MxFirst signal is: \[ \text{Latency} = \left( \left( \text{Ck10Count} + 1 \right) \bmod 2 \right) + 6 \]

Where:
- Latency is given in CK10M cycles. It begins at the first Ck10M rising edge which follows the Sync
  falling edge
- Ck10Count is the value of a CK10M counter at the falling edge of SYNC

Figure 2 zoom on the readout start. After a latency of 6 or 7 CK10M cycles, Mxfirst goes active and the
analogue signal generated in respect with the serial format.

Figure 3 zoom on the transition between 2 consecutive rows of the same frame. The markers are clearly showed.
Figure 4 shows the end of the last row readout followed by the first row of the next frame.
Figure 5 shows the alternate option of the MxFirst signal. It is permanently running, being active high on the first maker. This option is set via the RoMode register.

Figure 1

Figure 2

End of 1st row readout 2nd row readout
3.6.2 Test mode readout

The initialisation phase if the test mode is the same than in the normal mode. But it has to be noticed than the LastCol and LastRow makers are unavailable because the test mode has nothing to deal with the matrix and its line and column addressing registers. For the same reason the MxFirst maker is unavailable in the “First Pixel of frame mode” but only continuous mode.
3.6.3 Main Signal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT RSTB Pulse Width</td>
<td>≥1 μS</td>
<td>Active Low, Asynchronous Power on Reset</td>
</tr>
<tr>
<td>JTAG TCK Frequency</td>
<td>10 MHz</td>
<td>Boundary Scan Clock</td>
</tr>
<tr>
<td>TMS Setup/Hold Time</td>
<td>~10 nS</td>
<td>Boundary Scan Control Signal</td>
</tr>
<tr>
<td>TDI Setup/Hold Time</td>
<td>~10 nS</td>
<td>Boundary Scan Serial Data In</td>
</tr>
<tr>
<td>READOUT CKRD Frequency</td>
<td>Up to 50 MHz</td>
<td>Readout Clock LVDS signal</td>
</tr>
<tr>
<td>CKRD Duty Cycle</td>
<td>50%</td>
<td></td>
</tr>
<tr>
<td>SYNC Setup/Hold Time</td>
<td>5 nS</td>
<td>Chip Initialisation, CMOS signal. Starts after falling edge on 1st CKRD sampling</td>
</tr>
<tr>
<td>Differential Current Buffer (1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Dynamic range</td>
<td>0.7 up to 1.2 V</td>
<td></td>
</tr>
<tr>
<td>Rise time</td>
<td>5 nS</td>
<td>@ 10-90%, for fully input dynamic range</td>
</tr>
<tr>
<td>Fall time</td>
<td>5 nS</td>
<td>Simulated with $Z_{load} = 2 \times 100 \text{ Ohm}$ and 2*5pF</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>245 MHz</td>
<td>@ -3 dB</td>
</tr>
<tr>
<td>Transconductance gain</td>
<td>5.8 mS</td>
<td></td>
</tr>
<tr>
<td>Output Current Range</td>
<td>-2.2; 2.2 mA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The differential current output buffer can be modelled as an ideal current source. Its performances in terms of raising and falling times are limited by its load’s time constant ($R_{load} \times C_{load}$)

Note 2: Simple source follower

3.7 ADC

3.7.1 ADC_SEL register

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Selected signal for the measure</th>
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</thead>
<tbody>
<tr>
<td>19</td>
<td>DAC V4FASTBUF1</td>
</tr>
<tr>
<td>18</td>
<td>DAC V4FASTBUF0</td>
</tr>
<tr>
<td>17</td>
<td>DAC V4REG9</td>
</tr>
<tr>
<td>16</td>
<td>DAC V4REG8</td>
</tr>
<tr>
<td>15</td>
<td>DAC V4REG7</td>
</tr>
<tr>
<td>14</td>
<td>DAC V4REG6</td>
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<td>13</td>
<td>DAC V4REG5</td>
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<tr>
<td>12</td>
<td>DAC V4REG4</td>
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<td>DAC V4REG1</td>
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<td>7</td>
<td>DAC VTEST1</td>
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<td>6</td>
<td>DAC VTEST0</td>
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<td>---------------</td>
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<td>VDDD Chip supply</td>
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<tr>
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<td>VMUX&lt;1&gt; Pad</td>
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<tr>
<td>0</td>
<td>VMUX&lt;0&gt; Pad</td>
</tr>
</tbody>
</table>
4 Pad Ring

The pad ring of the chip is built with
- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 7 functional independent parts
- Read out analogue output<1> & analogue supplies
- CMOS JTAG & digital supplies
- LVDS read-out drivers
- Digital read-out control & digital supplies
- Read out analogue output<0> & analogue supplies
- Test ADC input signals
- Test ADC control signals & supplies

4.1 MimoStar3 Pad Ring and Floor Plan View

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Foundry submission information
Mimostar3 has been designed in AMS C35B4O1 CMOS 0.35 μm epitaxial and opto process with 2 poly and 4 metal layers.
The Process Design Kit V3.70 has been provided by CMP
CAD tools are CADENCE DFII 5.0 with DIVA and ASSURA rules
The chip has been submitted in an engineering run via CMP the June 2006

4.2 Pad List
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<th>Pad</th>
<th>Name</th>
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<th>PadType</th>
<th>Function for the chip</th>
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<td>Ground periphery &amp; core</td>
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<td>DIRECTPAD</td>
<td>Temperature probe output</td>
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### Pad ring segment 2 – P_D1

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<td>JTAG Control Signal</td>
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<td>94</td>
<td>CKRN</td>
<td>LVDS In -</td>
<td>Full Custom</td>
<td>Readout Clock Signal</td>
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<td>95</td>
<td>CKRP</td>
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### Pad ring segment – P_D2

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### Pad ring segment – P_A2

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<td>Ground periphery &amp; core</td>
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