MimoStar2
User Manual

MimoStar2 User Manual

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Mimo★

Document history		
Version	Date	Description
1.1	January 2006	Bias synthetic block diagram added
1.0	August 2005	MimoStar2 First Version
0.0		Based on MimoStar1 Version

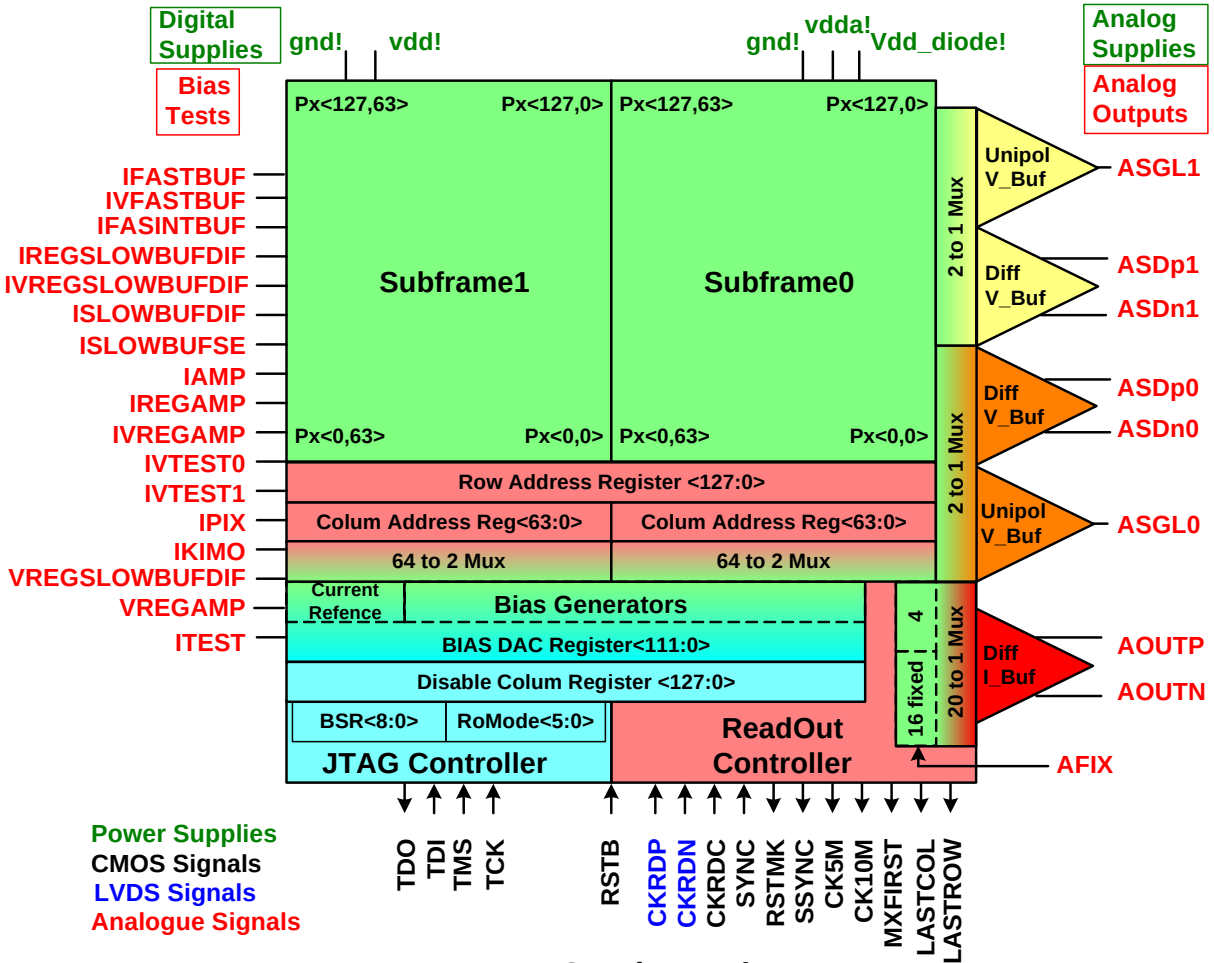
MimoStar chip		
Version	Date	Description
2	Submitted:June 05	AMS 035 Version
1	Submitted July 04	TSMC 025 Version

1 Introduction

Mimostar2, an enhanced version of MimoStar1, has been designed in C35B4O1, the AMS 0.35 µm opto process. Like MimoStar1, it is a Monolithic Active Pixel Sensor prototype dedicated to vertex particle tracking in a future update of the STAR vertex detector. The matrix is composed by 128 x 128 pixels of 30 µm pitch and based on self biased diode architectures. It is organised in 2 matrices, or subframes, of 128 lines x 64 columns, accessed in parallel during the readout. Each matrix contains a different pixel architecture, a so called "standard pixel" already designed and tested and a new structure which should meet the radiation tolerance and the low leakage current requirements. Actually Mimostar2 is a downsized prototype which emulates the final circuit. This one is foreseen with 640 x 640 pixels organised in 10 subframes of 640 lines x 64 columns.

The addressing of each subframe is sequential and starts from the upper left pixel up to the lower right pixel. Analogue data are extracted via a selectable set of analogue buffers. One can choose between the parallel outputs or the serial output.

- Parallel output
  Two types of output voltage buffers are provided; unipolar and differential Each subframe has its dedicated buffer running at a readout speed from 5 up to 10 MHz.
- Serial output
  The serialised, multiplexed, data of the 2 pixel subframes are driven out via a differential current output buffer. Its readout speed should be from 50 up to 100 MHz.



MimoStar2 functional view
Does not correspond to the floorplan; neither for the core, neither for the pad ring

MimoStar2 is very simple to operate:

- Power On Reset or Reset on RSTB pad
- Setup of the chip
  It is performed with programmable registers accessed via an embedded slow control interface. It consists to:
  - Load the DACs which bias the analogue blocks
  - Select the readout clock source among the LVDS or the CMOS input
  - Select the serial or the parallel readout
    - For parallel readout, select differential or single ended analogue output buffer
  - The default setup after power on reset is
    - CMOS input readout clock
    - 10 MHz readout clock
    - Parallel differential output buffer
- Readout of the chip
  - The readout starts when the input "SYNC" token signal is sampled by the readout clock. It happens at the first rising edge of the "10 MHz equivalent" clock which follows the SYNC falling edge.
  - After a latency of 4 "10 MHz equivalent" clock cycles, the analogue signals appear on the selected output(s) buffer(s)
  - Digital maker outputs are available for the control of the readout process
  - Pixels are sequentially read out in a specific order explained later in the document
  - Successive pixel frames are read until the readout clock is stopped

A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

2 Control Interface

The control interface of MimoStar2 complies with the Boundary Scan, JTAG, IEEE 1149.1 Rev 1999 standard. It allows the access to the internal registers of the chip like the bias register and the readout mode selection register.
On Power-On-Reset, an internal reset for the control interface is generated. The finite state machine of the Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the ID register is selected.

Remarks on the Differential Current Output Buffers:
MimoStar2 has been designed in order to be fully adjustable via the control interface. Nevertheless the AFIX voltage level still needs to be fixed via a pad (see pad listing table).

2.1 *JTAG Instruction Set*

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of the desired data register to access.

Instruction	**5 Bit Code$_{16}$**	**Selected Register**	**Notes**
EXTEST	01	BSR	JTAG mandatory instruction
HIGHZ	02	BYPASS	JTAG optional instruction
INTEST	03	BSR	JTAG optional instruction
CLAMP	04	BYPASS	JTAG optional instruction
SAMPLE_PRELOAD	05	BSR	JTAG mandatory instruction
BIAS_GEN	10	BIAS register	User instruction
DIS_COL	11	Disable Columns	User instruction
ID_CODE	12	(1)	Reserved - JTAG optional instruction
NU1	13	(1)	Reserved, Not Used
NU2	14	(1)	Reserved, Not Used
NU3	15	(1)	Reserved, Not Used
NU4	16	(1)	Reserved, Not Used
RO_MODE	17	Read Out Mode	User instruction
BYPASS	1F	BYPASS	JTAG mandatory instruction

(1) Instruction codes implemented but not the corresponding registers. To be fixed in the next version.

2.2 JTAG Register Set

JTAG registers are implemented with a Capture/Shift register and an Update register. JTAG standard imposes that the last significant bit of a register is downloaded/shifted first.

Register Name	Size	Access	Notes
INSTRUCTION REG	5	R/W	Instruction Register
BYPASS	1	R Only	
BSR	10	R/W	
BIAS_GEN	112	R/W	Previous value shifted out during write
RO_MODE	6	R/W	Previous value shifted out during write
DIS_COL	128	R/W	
ID_REG, NU1, NU2, NU3, NU4	0	-	Not implemented. For future use

2.2.1 Instruction Register

The Instruction register is a part of the Test Access Port Controller defined by the IEEE 1149.1 standard. The Instruction register of MimoStar2 is 5 bits long. On reset, it is set with the ID_CODE instruction. When it is read the 2 last significant bits are set with the markers specified by the standard, the remaining bits contain the current instruction.

X	**X**	**X**	**1**	**0**

2.2.2 Bypass Register

The Bypass register consists of a single bit scan register. It is selected when its code is loaded in the Instruction register, during some actions on the BSR and when the Instruction register contains an undefined instruction.

2.2.3 Boundary Scan Register

The Boundary Scan Register, according with the JTAG instructions, tests and set the IO pads. The MimoStar2 BSR is 9 bits long and allows the test of the following input and output pads

Bit #	Corresponding Pad	Type	Signal	Notes
9	LVDS CkRdP/CkRdN	Inputs	CkRd	Resulting CMOS signal after LVDS Receiver
8	CMOS CkRd	Inputs	CkRd	
7	CMOS Sync	Inputs	Sync	
6	SSync	Output	SSync	
5	Ck5M	Output	Ck5M	
4	Ck10M	Output	Ck10M	
3	RstMk	Output	RstMk	
2	LastRow	Output	LastRow	
1	LastCol	Output	LastCol	
0	MxFirst	Output	MxFirst	

2.2.4 BIAS_DAC Register

The BIAS_DAC register is 112 bits large; it sets simultaneously the 14 DAC registers.
As show bellow these 8-bit DACs set voltage and current bias.
After reset the register is set to 0, a value which fixes the minimum power consumption of the circuit.
The current values of the DACs are read while the new values are downloaded during the access to the register.
An image of the value of each DAC can be measured on its corresponding test pad.

Bit range	DAC #	DAC Internal Name	DAC purpose	Corresponding Test Pad
111-104	DAC13	IKIMO	External circuit monitoring	IKIMO
105- 96	DAC12	I4PIX	Pixel source follower bias	IPIX
95- 88	DAC11	V4TEST1	Test Level, emulates a pixel output	IVTEST1
87- 80	DAC10	V4TEST0	IDEM	IVTEST0
79- 72	DAC9	V4REG1	Voltage regulator voltage bias of the	IVREGAMP

			column amplifier (G3 &5)	
71- 64	DAC8	I4REG1	Idem	IREGAMP
63- 56	DAC7	I4AMP	Bias of the group of column amplifiers	IAMP
55- 48	DAC6	I4BUF10SE	Bias of the single ended parallel voltage Output Buffer	ISLOWBUFSE
47- 40	DAC5	I4BUF10DIF	Bias of the differential parallel voltage Output Buffer	ISLOWBUFDIF
39- 32	DAC4	V4REG2	Voltage regulator bias of the differential parallel Output Buffer	IVREGSLOWBUFDIFF
31- 24	DAC3	I4REG2	Idem	IREGSLOWBUFDIFF
23- 16	DAC2	I4FASTINTBUF	Bias of the fast Intermediate Buffer	IFASTINTBUF
15- 8	DAC1	V4FASTBUF	Bias of the differential current Output Buffer	IVFASTBUF
7- 0	DAC0	I4FASTBUF	Idem	IFASTBUF

2.2.5 RO_Mode Register

The RO_Mode register is 6 bits large; it allows the user to select the type of readout for the chip.

- Test mode versus normal mode
- Parallel analogue outputs versus serial output
- Amplification gain of 3 versus 5 for the serial analogue output buffer

Bit #	Bit Name	Purpose	Default value	
5	SelLVDS	Select LVDS versus CMOS input readout clock pad	0	CMOS input
4	SelMux	On MxFirst output, select MuxFirst signal or First_Pixel_of_First_Frame signal	1	MuxFirst Signal, active See § 3.4 Readout
3	EnaGain3	Select gain 3 for the serial differential output buffer	0	Gain 5
2	Ena10MHz	Select between the parallel readout or the serial readout	1	10 MHz Clock selected →Parallel analogue outputs
1	SelPSgl	Select between differential or single ended parallel analogue output	0	Differential voltage output buffer
0	EnaTstCol	Test Mode: Select the 2 Test Levels, IVTEST1 and IVTEST0, which emulate a pixel output	0	Normal mode

2.2.6 DIS_COL Register

The DIS_COL register is 128 bit wide. The purpose of this register is to disable the column current sources if a short circuit is suspected on a specific column. During the readout, even if a current source is disabled the corresponding column is selected, i.e. no columns are skipped. Obviously, the signal of the corresponding pixel has not signification.

The default value of the DIS_COL register is 0; it means that all current sources can be activated by the readout logic. Setting a bit to 1 disables the corresponding current source. In MimoStar1, the column<127> is on the left hand side while column<0> is on the right hand side. The organisation of the chip in 2 subframes of 64 columns has no matter to do with the DIS_COL register.

127 (Msb)	**0 (Lsb)**
DisCol<127>	**DisCol<0>**

2.2.7 DEV_ID Register

The Device Identification register is not implemented yet. When selected by the ID_CODE instruction or after a reset no real data are shifted, a 0 value takes place on TDO, the JTAG serial output of the chip.

3 Running MimoStar2

The following steps describe how to operate Mimostar2

3.1 After reset

On RSTB active low signal:

- All BIAS registers are set to the default value, i.e. 0
- DIS_COL is set to 0, i.e. all columns are selected
- RO_Mode is set to the binary value 10100 (see default setting)
- JTAG state machine is in the Test-Logic-Reset state
- JTAG ID_CODE instruction is selected

Then the bias register has to be loaded.
The same for the RO_MODE and DIS_COL registers if the running conditions differ from defaults.
Finally the readout can be performed either in normal mode or in test mode.

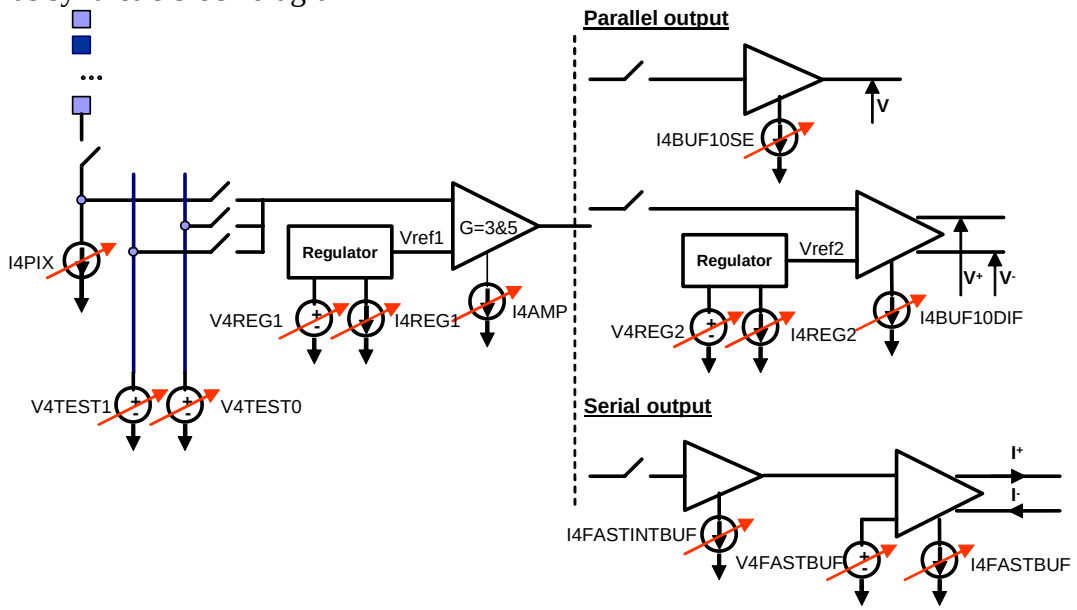
3.2 Biasing MimoStar2

The BIAS_DAC register has to be loaded before operating MimoStar2.
The 14 DACs constituting this register are built with the same 8 bits DAC current generator which has a 1 µA resolution. Specific interfaces like current mirror for current sourcing or sinking and resistors for voltages, customise each bias output. The following table shows the downloaded codes which set the nominal bias.

Internal DAC Name	Simulation			Resolution	Range	Experimental	
	$Code_{16}$ - $Code_{10}$	DacInternal current-µA	Output value			$Code_{16}$ - $Code_{10}$	Output value
IKIMO	64-100	100	1 V	10 mV	From 0 up to 2.55 V	64-100	1 V
I4PIX	1E-30	30	30 µA	1 µA	From 0 up to 255 µA	1E-30	30 µA
V4TEST1	C3–195	195	1.95 V	10 mV	From 0 up to 2.55 V	C3–195	1.95 V
V4TEST0	B9–185	185	1.85 V	10 mV	From 0 up to 2.55 V	B9–185	1.85 V
V4REG1(Note 1)	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	**32–50**	**2.80 V**
I4REG1	21–33	33	33 µA	1 µA	From 0 up to 255 µA	21–33	33 µA
I4AMP	64–100	100	100 µA	1 µA	From 0 up to 255 µA	64–100	100 µA
I4BUF10SE	32–50	50	50 µA	1 µA	From 0 up to 255 µA	32–50	50 µA
I4BUF10DIF	14–20	20	20 µA	1 µA	From 0 up to 255 µA	14–20	20 µA
V4REG2(Note2)	23–35	35	2.95 V	10 mV	From 3.3 down to 0.75 V	23–35	2.95 V
I4REG2	21–33	33	33 µA	1 µA	From 0 up to 255 µA	21–33	33 µA
I4FASTINTBUF	64–100	100	100 µA	1 µA	From 0 up to 255 µA	64–100	100 µA
V4FASTBUF	5C–92	92	0.92 V	10 mV	From 0 up to 2.55 V	5C–92	0.92 V
I4FASTBUF	28–40	40	40 µA	1 µA	From 0 up to 255 µA	28–40	40 µA

Note1: Vref1 ~= V4REG1 – 1V; Note2: Vref2 ~= V4REG2 – 1V

Bias synthetic block diagram



3.3 Setting the Readout_Mode Register

If the desired operating mode does not correspond to the default one, set the Readout_Mode register following the §2.2.5 informations.

3.4 Readout

3.4.1 Signal protocol

Ones JTAG registers have been loaded, the readout of MimoStar2 may initiate with the following signal protocol:

- The readout clock is started. This allows the CK10M output pad to generate a 10 MHz clock. This clock follows the input clock with a 1/10 ratio if the 100 MHz is selected.
- The SYNC signal is set.
- The readout starts at the first rising edge of CK10M of after SYNC signal disappears.
- Signal markers allow the readout monitoring and the analogue data sampling:
    - RstMk maker confirms the internal reset of the readout logic.
    - SSync marker shows that the readout starts.
    - 4 extra CK10M clock cycles, after SYNC sampling, are necessary before the first pixel analogue signal appears on the selected output(s).
    - The MxFirst digital signal helps for a better sampling of the analogue output signals. The way it acts is set by the RO_Mode[4] bit.
        - RO_Mode[4] = 0: MxFirst is active only on the first pixel oft the first frame
        - RO_Mode[4] = 1: MxFirst is active on each pixel change on the parallel analogue output i.e. it is a10 MHz periodic signal.
          Used with the 100 MHz serial mode (see serial data format bellow), its period shows when one pixel index has been read in all the subframes (2 real + 8 virtual).
    - LastCol is active when the last column of the current row is selected
    - LastRow is active when the last row of the frame is selected
    - Ck5MHz output shows the internal clock running as long as input clock (10 or 100MHz) is running.

3.4.2 Successive frames and resynchronisation

Successive pixel frames are read until the readout clock is stopped.
A frame resynchronisation can be performed at any time by setting up the "SYNC" token again.

3.5 Analogue Data Format

Two types of signal can be generated in serial or in parallel mode

- Normal pixel signal
- Test signal.

This gives 4 different formats of data

- Normal Serial Format
- Normal Parallel Format
- Test Parallel Format
- Test Serial Format

3.5.1 Normal data format

In order to improve the readout speed Mimostar2 is organized in subframes, i.e. 2 subframes for this current prototype and 10 for the foreseen full-size version.
During the readout, the 2 subframes of Mimostar2 are accessed in parallel. For each subframe the addressing is done row by row, each pixel is accessed sequentially from the left side to right side. Each row contains 2 dummy pixels, and 64 active pixels. During the readout one can use the adjustable level of the 2 dummy pixels as a pattern recogniser. If the pixel coordinate format is specified as Px<Line, Column>, then for each subframe, the upper left pixel is Px<127, 63> while the lower right is Px<0, 0> and the dummy pixels of each beginning row are named Dp1 and Dp0.

3.5.1.1 Parallel Mode

There is one output buffer per subframe: thus the Normal Parallel Mode data stream format for each output is:

```
Dp1, Dp0, Px<127,63>, Px<127,62>,. . ., Px<127,0>
Dp1, Dp0, Px<126,63>,.Px<126,62>,. . ., Px<126,0>
. . . . . . . . . . . . . . . . . . . . . . . . .
Dp1, Dp0, Px<  1,63>,.Px<  1,62>,. . ., Px<  1,0>
Dp1, Dp0, Px<  0,63>,.Px<  0,62>,. . ., Px<  0,0>
```

3.5.1.2 Serial Mode

The serial mode consists to read successively one pixel of each subframe and then turning back to the first subframe in order to read its next pixel. Even if Mimostar2 is a downsized prototype of 2 subframes the serial readout strategy has been maintained for 10. This implies for the serial format 8 dummy values on 10 analogue data. These dummy values are fixed via the AFIX pad.

For Mimostar2 the left hand side subframe is named Sf1 and the right hand side is Sf0 while the dummy values generated in place of the 8 non-existing subrames are named from Dv7 to Dv0.. Thus the normal data stream in serial mode has the following format:

```
 Sf1Dp1,         Sf0Dp1,         Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Dp0,         Sf0Dp0,         Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<127,63>, Sf0Px<127,63>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<127,62>, Sf0Px<127,62>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
Sf1Px<127, 0>, Sf0Px<127, 0>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Dp1,         Sf0Dp1,         Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Dp0,         Sf0Dp0,         Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<126,63>, Sf0Px<126,63>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<126,62>, Sf0Px<126,62>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
Sf1Px<126, 0>, Sf0Px<126, 0>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
Sf1Dp1,         Sf0Dp1,         Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Dp0,         Sf0Dp0,         Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<  0,63>, Sf0Px<  0,63>,.Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
Sf1Px<  0,62>, Sf0Px<  0,62>,.Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
Sf1Px<  0, 0>, Sf0Px<  0, 0>, Dv7, Dv6, Dv5, Dv4, Dv3, Dv2, Dv1, Dv0,
```

3.5.2 Test data format

During the test mode the pixel matrix is not connected to the multiplexing electronic. In place of it, two test levels V4TEST1 (V1), V4TEST0 (V0) are available. They emulate two pixel level outputs. Actually these levels correspond to those of Dummy Pixel 1 and Dummy Pixel 0. They are adjustable via 2 DACs. Even and odd columns are alternatively connected to one of them. This pattern allows seeing the output signal changing and emulates the readout shift from one column of pixel to the other column of pixel.

3.5.2.1 Parallel Mode

There is one output buffer per subframe: thus the Test Parallel Mode data stream format per output is:

Subframe 1: **V1, V0, V0, V1**, V1, V0, V0, V1 . . .

Subframe 0: **V0, V1, V1, V0**, V0, V1, V1, V0 . . .

3.5.2.2 Serial Mode

Test data stream in serial mode has the following format:

Sf1V1, Sf0V0, Sf1V0, Sf0V1, Sf1V0, Sf0V1, Sf0V1, Sf0V0,
Sf1V1, Sf0V0, Sf1V0, Sf0V1, Sf1V0, Sf0V1, Sf0V1, Sf0V0 . . .

3.6 MimoStar2 Chronogram

The following chronograms describe typical access to Mimostar2; Reset, JTAG download sequence and then the readout of the chip. This one starts with the initialisation phase followed by the successive row readouts as showed in the zoom.

3.6.1 Serial Readout

Figure 1 show a typical readout in serial mode. After Reset and JTAG settings, one can see the readout oft the first pixel row readout followed by successive rows readout marked by the LastCol signal. Finally the LastRow signal active high indicates that the readout of the last row of the frame is performed.

Figure 2 zoom on the readout start. One can see that it starts after a latency of 4 CK10M cycles following the sampling of SYNC low by this clock. Mxfirst goes active and the analogue signal generated in respect with the serial format.

Figure 3 zoom on the transition between 2 consecutive rows. The 2 dummy pixels of each subframes are clearly showed.

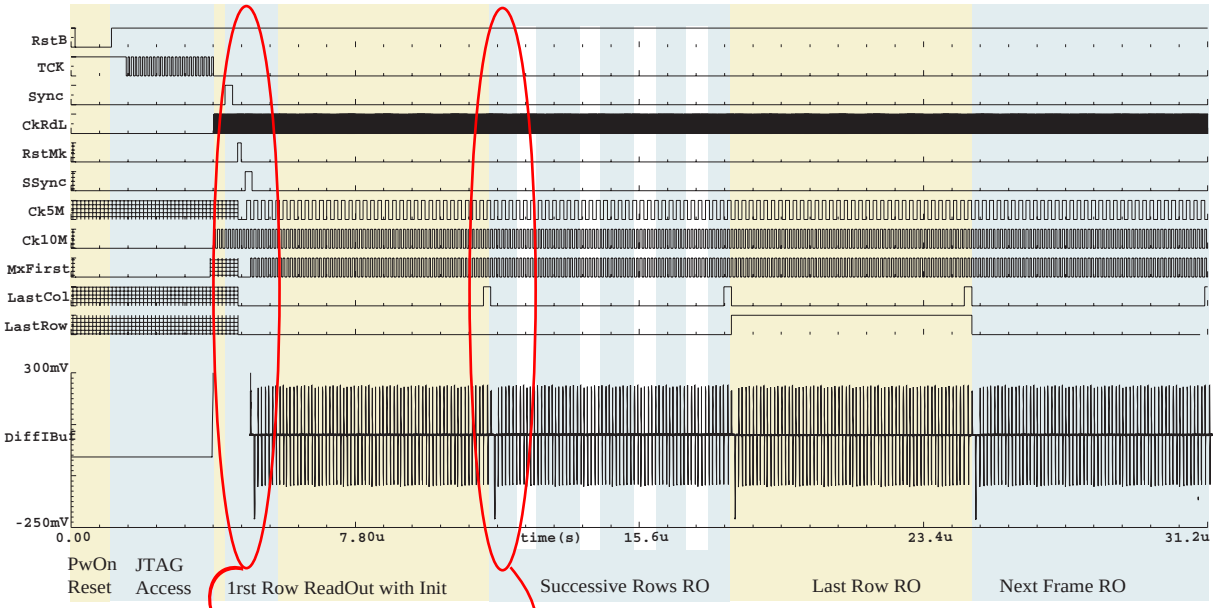


Figure 1

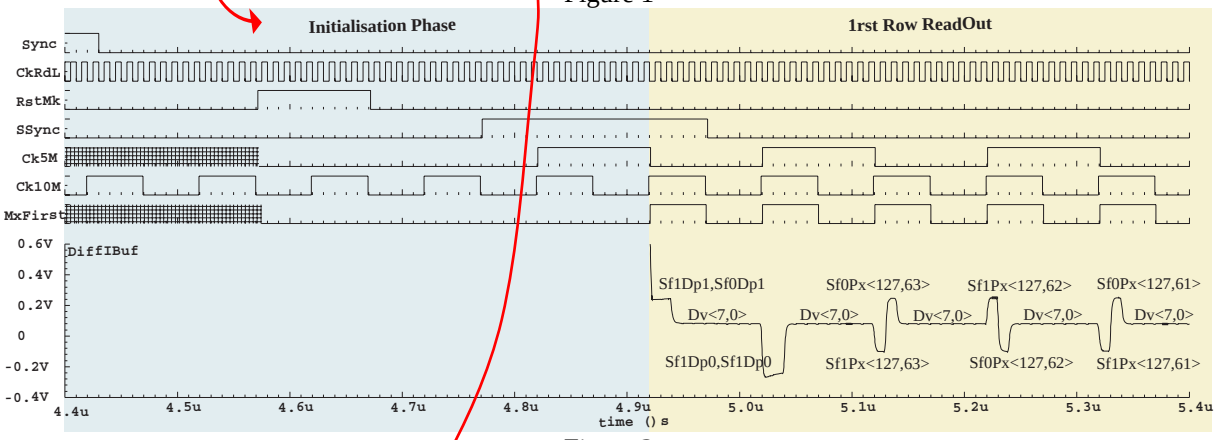


Figure 2

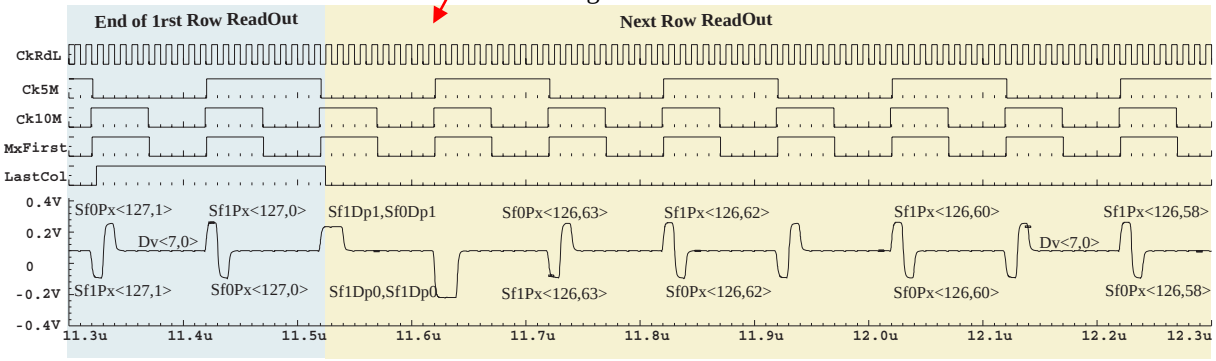


Figure 3

3.6.2 Parallel Readout

Figure 1 show the beginning of a typical readout in parallel mode. After Reset and JTAG settings, one can see the readout oft the first pixel row readout followed the successive one indicated by the LastCol signal.. The parallel analogue outputs are showed. One can distinguish the 2 dummy pixels at the beginning of each row readout.. This is clearer in the zoom of figure 2

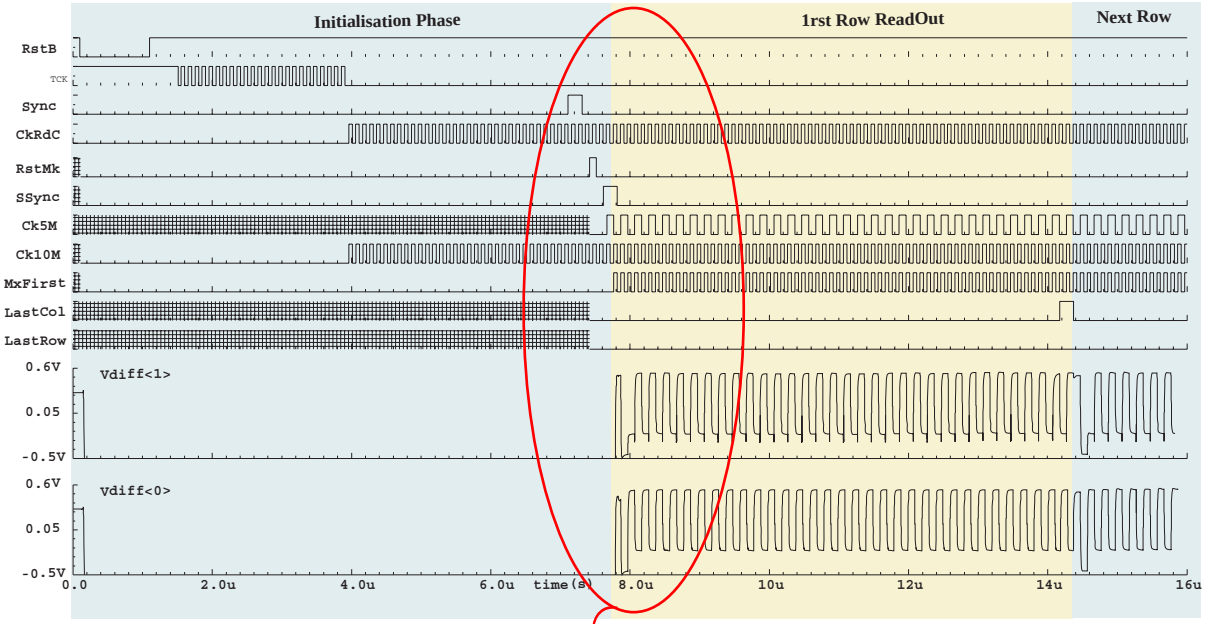


Figure 1

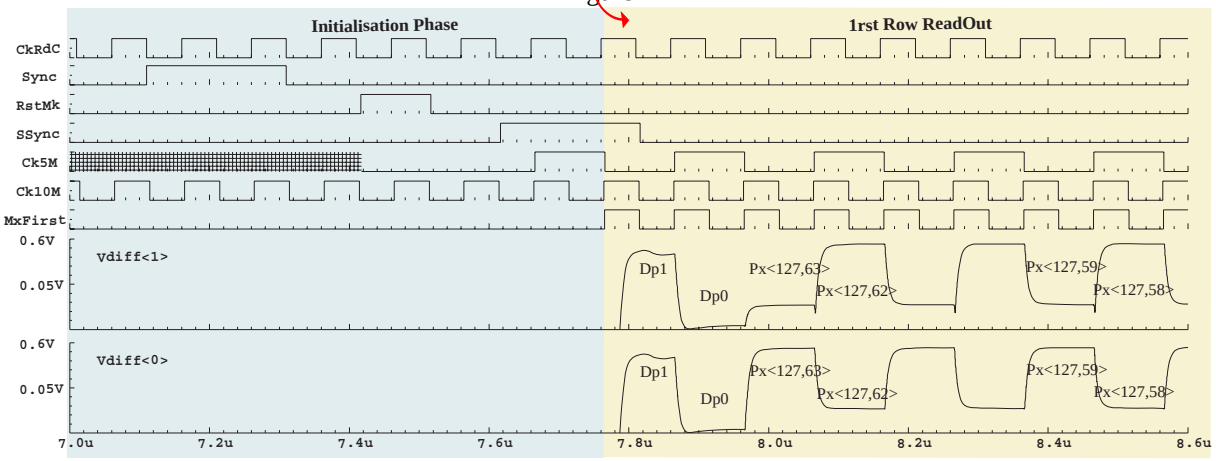


Figure 2

3.6.3 Main Signal Specifications

	Parameter	Typical Value	Notes
INIT	RSTB Pulse Width	>1 µS	Active Low, Asynchronous Power on Reset
JTAG	TCK Frequency	10 MHz	Boundary Scan Clock
	TMS Setup/Hold Time	~10 nS	Boundary Scan Control Signal
	TDI Setup/Hold Time	~10 nS	Boundary Scan Serial Data In
READOUT	CKRD Frequency	Up to 100 MHz	Readout Clock LVDS signal
	CKRD Frequency	Up to 10 MHz	Readout Clock CMOS signal
	CKRD Duty Cycle	50%	
	SYNC Setup/Hold Time	5 nS	Chip Initialisation, CMOS signal. Starts after falling edge on 1rst CKRD sampling
Differential Current Buffer (1)	Input Dynamic range	0.7 up to 1.2 V	
	Rise time	5 nS	@ 10-90%, for fully input dynamic range Simulated with Z_{load} = 2*100 Ohm and 2*5pF
	Fall time	5 nS	
	Bandwidth	245 MHz	@ -3 dB
	Transconductance gain	5.8 mS	
	Output Current Range	-2.2; 2.2 mA	
AFIX	Bias value	1.5 V	Serial Output Buffer Dummy Data
Differential Voltage Buffer	Rise time	10 nS	@ 10-90%
	Fall Time	10 nS	
	Bandwidth	40 MHz	@ -3 dB
	Capacitance load	1 pF	
Unipolar Buffer (2)	Rise/ fall time	6 nS	@ 10-90%, Full analogue chain simulated with load capacitance of 10pF
	Fall Time	7 nS	
	Capacitance load	10 pF	

Note 1: The differential current output buffer can be modelled as an ideal current source. Its performances in terms of raising and falling times are limited by its load's time constant (R_{load} x C_{load})

Note 2: Simple source follower

4 Pad Ring

The pad ring of Mimlostar2 is build with

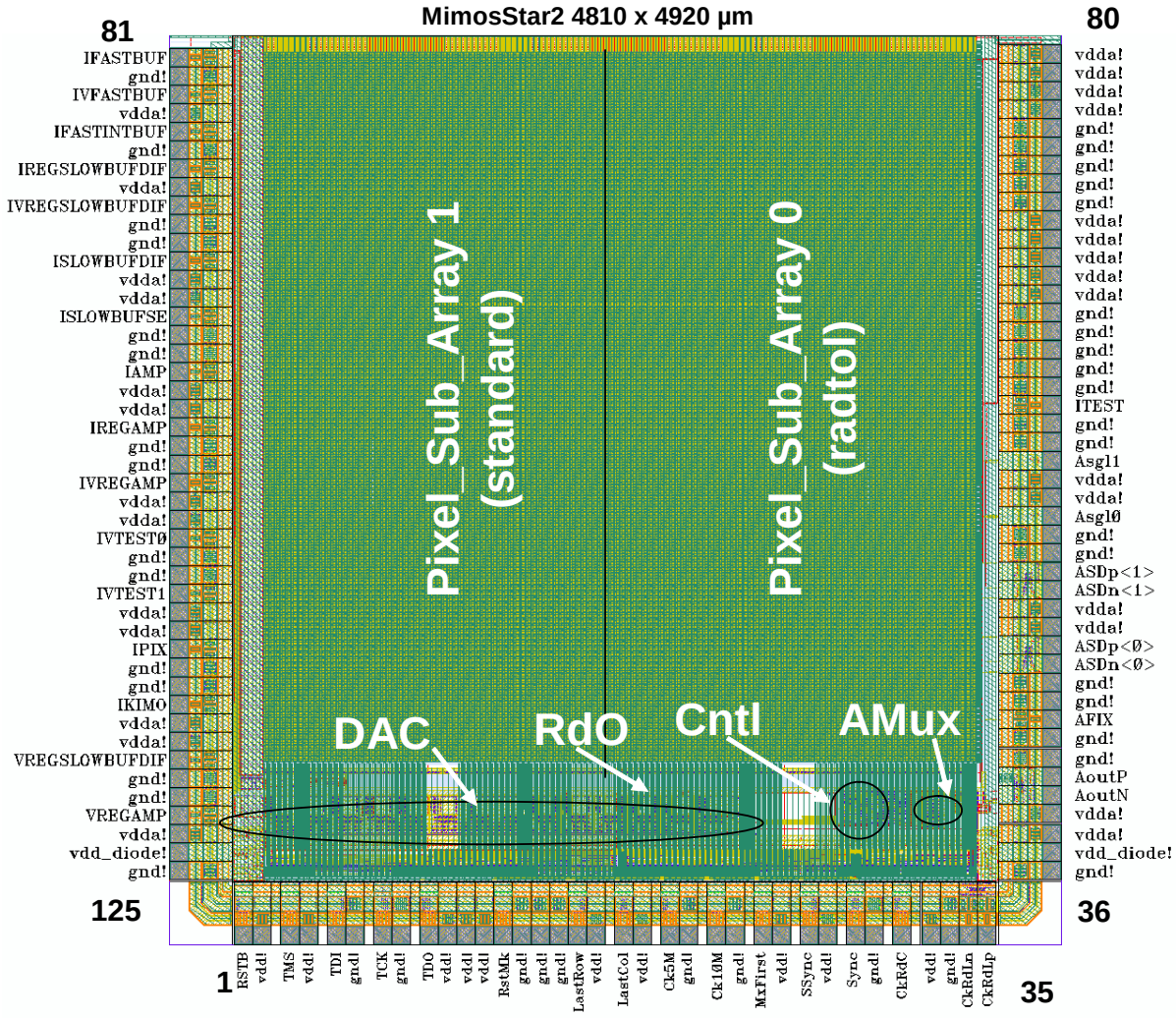
- Pads full custom designed for some of the analogue signals and power supplies
- Pads from the AMS library for the digital signals and power supplies

The pad ring is split in 6 functional independent parts

- CMOS JTAG and Read Out Control
- LVDS Read Out Drivers
- Analogue Core Supplies
- Read Out Analogue Outputs
- Test Structure pads, Mimostar1 independent
- Bias Test

Each part has its own supply pads.

4.1 MimoStar2 Pad Ring and Floor Plan View



Total Pads =125 - Supply Pads: Gnd =42, Vdd = 9, AVdd=28

Foundry submission information

Mimostar2 has been designed in AMS C35B4O1 CMOS 0.35 µm epitaxial and opto process with 2 poly and 4 metal layers.

The Process Design Kit V3.60 has been provided by CMP

CAD tools are CADENCE DFII 5.0 with DIVA and ASSURA rules

The chip has been submitted in a Multi Chip Run via CMP the 25 June 2005 in the run # A35C5-4.

4.2 Pad List

The bonding of the power supply pads specified in red colour is mandatory

Horizontal Bottom Side				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
1	RSTB	Schmitt-Trigger Input Buffer, Pull Up	ISUP	Asynchronous Active Low Reset
2	VDD	Pad supplying the output buffers	VDD3OP	3.3 V
3	TMS	CMOS Input Buffer, Pull Up	ICUP	JTAG Control Signal
4	VDD	Core logic and periphery cells supply	VDD3RP	3.3 V periphery cells only
5	TDI	CMOS Input Buffer, Pull Up	ICUP	JTAG Serial Data In
6	GND	Pad supplying the output buffers	GND3OP	Ground
7	TCK	CMOS Clock Input Buffer, 2 mA	ICCK2P	JTAG Clock
8	GND	Core logic and periphery cells supply	VDD3RP	Ground periphery cells only
9	TDO	Tri-State Output Buffer, 4 mA	BT4P	JTAG Serial Data Out
10	VDD	Core logic and periphery cells supply	VDD3RP	**3.3 V periphery & core**
11	VDD	Core logic and periphery cells supply	VDD3RP	**3.3 V periphery & core**
12	VDD	Pad supplying the output buffers	VDD3OP	**3.3V**
13	RstMk	Tri-State Output Buffer, 2 mA	BT2P	Readout Reset Marker
14	GND	Core logic and periphery cells supply	VDD3RP	**Ground periphery & core**
15	GND	Core logic and periphery cells supply	VDD3RP	**Ground periphery & core**
16	GND	Pad supplying the output buffers	GND3OP	**Ground**
17	LastRow	Tri-State Output Buffer, 2 mA	BT2P	Last Row Maker
18	VDD	Core logic and periphery cells supply	VDD3RP	3.3 V periphery cells only
19	LastCol	Tri-State Output Buffer, 2 mA	BT2P	Last Column Marker
20	VDD	Pad supplying the output buffers	VDD3OP	3.3 V
21	CK5M	Tri-State Output Buffer, 2 mA	BT2P	5 MHz Clock Out
22	GND	Core logic and periphery cells supply	GND3RP	Ground periphery cells only
23	CK10M	Tri-State Output Buffer, 2 mA	BT2P	10 MHz Clock Out
24	GND	Pad supplying the output buffers	GND3OP	Ground
25	MxFirst	Tri-State Output Buffer, 2 mA	BT2P	Subframes odd pixel selection
26	VDD	Core logic and periphery cells supply	VDD3RP	3.3 V periphery cells only
27	SSnc	Tri-State Output Buffer, 2 mA	BT2P	Readout Synchro. Start Marker
28	VDD	Pad supplying the output buffers	VDD3OP	3.3 V
29	Sync	CMOS Input Buffer	ICP	Readout Input token
30	GND	Core logic and periphery cells supply	GND3RP	Ground periphery cells only
31	CkRdC	CMOS Input Buffer, Pull Down	ICDP	Readout Clock Signal
32	VDD	LVDS Pad Supply	AVDDALLP	**3.3V for LVDS Pad**
33	GND	LVDS Pad Ground	AGNDALLP	**Ground for LVDS Pad**
34	CkRdLn	LVDS In-	Full Custom	Readout Clock Signal
35	CkRdLp	LVDS In+	Full Custom	

Vertical Right Hand Side				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
36	GND		AGNDALLP	**Analogue Core Ground**
37	Vdd-Diode	Direct Pad, no protections	Full Custom	**Pixel Diode Bias, 3.3V**
38	VDDA	Analogue Supply	AVDDALLP	**Analogue Core Supply**
39	VDDA	Analogue Supply	AVDDALLP	**Diff. Buffer Voltage Supply**
40	AoutN	Empty pad with embedded buffer	Full Custom	Serial Differential Current Output Buffer
41	AoutP		Full Custom	
42	GND	Analogue Gnd	AGNDALLP	**Diff. Buffer Ground Supply**
43	GND	Analogue Gnd	AGNDALLP	Analogue Pad Ring Gnd
44	AFIX	Analog I/O pad, 0 Ω serial resistor.	APRIOP	Serial Output Buffer Dummy Data
45	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Ring Gnd
46	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Ring Gnd
47	ASDn<0>	Empty pad with embedded buffer	Full Custom	Differential parallel output<0>
48	ASDp<0>		Full Custom	
49	VDDA	Analogue Core Supply	AVDDALLP	Analogue Pad Ring Supply
50	VDDA	Analogue Core Supply	AVDDALLP	Analogue Pad Ring Supply
51	ASDn<1>	Analogue voltage Out-	Full Custom	Differential parallel output<1>
52	ASDp<1>	Analogue voltage OutP+	Full Custom	
53	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
54	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
55	Asgl0	Empty pad with embedded buffer	Full Custom	Analogue Single Ended Output
56	VDDA	Analogue Core Supply	AVDDALLP	VDDA
57	VDDA	Analogue Core Supply	AVDDALLP	VDDA
58	Asgl0	Empty pad with embedded buffer	Full Custom	Analogue Single Ended Output
59	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
60	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
61	ITEST	Analog I/O pad, 0 Ω serial resistor.	APRIOP	Internal Current Ref Source Test
62	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
63	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
64	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
65	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
66	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
67	VDDA	Analogue Core Supply	AVDDALLP	VDDA
68	VDDA	Analogue Core Supply	AVDDALLP	VDDA
69	VDDA	Analogue Core Supply	AVDDALLP	VDDA
70	VDDA	Analogue Core Supply	AVDDALLP	VDDA
71	VDDA	Analogue Core Supply	AVDDALLP	VDDA
72	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
73	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
74	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
75	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
76	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
77	VDDA	Analogue Core Supply	AVDDALLP	VDDA
78	VDDA	Analogue Core Supply	AVDDALLP	VDDA
79	VDDA	Analogue Core Supply	AVDDALLP	VDDA
80	VDDA	Analogue Core Supply	AVDDALLP	VDDA

Vertical Left Hand Side				
Pad	**Name**	**Pad General Function**	**PadType**	**Function for the chip**
81	IFASTBUF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
82	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
83	IVFASTBUF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
84	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
85	IFASTINTBUF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
86	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
87	IREGSLOWBUFDIF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
88	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
89	IVREGSLOWBUFDIF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
90	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
91	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
92	ISLOWBUFDIF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
93	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
94	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
95	ISLOWBUFSE	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
96	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
97	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
98	IAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
99	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
100	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
101	IREGAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
102	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
103	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
104	IVREGAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
105	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
106	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
107	IVTEST0	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
108	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
109	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
110	IVTEST1	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
111	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
112	VDDA	Analogue Pad Supply	AVDDALLP	VDDA
113	IPIX	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
114	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
115	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
116	IKIMO	Analog I/O pad, 0 Ω serial	APRIOP	Gen Purpose DAC Output
117	VDDA	Analogue Core Supply	AVDDALLP	VDDA
118	VDDA	Analogue Core Supply	AVDDALLP	VDDA
119	VREGSLOWBUFDIF	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
120	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
121	GND	Analogue Pad Gnd	AGNDALLP	Analogue Pad Gnd
122	VREGAMP	Analog I/O pad, 0 Ω serial	APRIOP	DAC Test Purpose Only
123	VDDA	Analogue Core Supply	AVDDALLP	**VDDA**
124	VDD_DIODE	Direct Pad, no protections	Full Custom	**Pixel Diode Bias, 3.3 V**
125	GND	Analogue Pad Gnd	AGNDALLP	**Analogue Pad Gnd**