Optimization of amplifiers for Monolithic Active Pixel Sensors
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Introduction
Semiconductor position sensitive detectors are used in high precision particle tracking and imaging applications. Moving electron-hole pairs created in a pixelized semiconductor volume induce a current at the electrodes. The signal current is amplified, processed and readout by the corresponding electronics. The peculiarity of Monolithic Active Pixel Sensors (MAPS) is that the front-end electronics is implemented in a standard CMOS technology substrate, which is used as sensitive volume, contrary to all other types like CCD, hybrid pixel detectors, 3D electronics detectors.

The advantage of MAPS is their low cost due to usage of standard CMOS technology and possibility to implement amplification and complex data processing in the same chip. Certainly this implies restrictions for the architecture of electronics in MAPS: the front-end amplifier which placed directly in the pixel sensitive volume can use only one type of MOS transistors, unless expensive technologies with isolated transistors have been utilized. In addition to this, usage of low resistivity (10-200Ω cm) substrate in the standard CMOS technology makes it possible to deplete only very small fraction of the detector sensitive volume, and the electron-hole pairs transport is dominated by thermal diffusion.

Objectives and possible solutions
The spatial resolution and tracking performances of MAPS are improved with increase of signal-to-noise ratio of amplifier. The objective is to develop in-pixel amplifier which achieves:
- maximum of signal-to-noise ratio for a given pixel pitch size and readout channel charge collection size
- minimum of power consumption
- small pixel-to-pixel performance variation due to CMOS process variation

In order to maximize signal-to-noise ratio one need to obtain higher amplifier gain. Standard common source schematics (left) can be used, however they have not sufficient voltage gain (< 5), when only nmos transistors has to be used in design:

\[ Gain = \frac{V_{out}}{V_{in}} = \frac{2\mu I}{g_{m} + g_{d} + g_{m} + g_{d}} \]

Special biasing with transistor M3 for the load transistor (M2) has been introduced, and the gain of the improved schematic (right) increases, due to the cancellation of \( g_{m} \) for frequencies larger than \( 1/g_{m} \). The AC gain of improved amplifier increases by about factor of two, but the DC operation point and DC gain are almost not changed, which makes circuit more resistant to CMOS process variation. In addition to this, negative feedback can be used to stabilize the operation point of the amplifier.

The low pass filter and diodes capacitances discharge time is very large, so there will be unwanted memorization of some fraction of signal, which however reduced by correlated double sampling (CDS). A better approach is to use time variant feedback, the DC operational point is set by short pulse (set). The advantage of this schematic its simplicity and even higher gain, the disadvantage is large crosstalk to the sensing diode (D1) from switch transistor (M3).

One can reduce the crosstalk by lowering down the controlling voltage pulse, or increasing the diode size and hence its capacitance. Each pixel has CDS circuit based on clamping technique: i.e. first sample is the amplifier output voltage stored on clamping capacitor, second sample is subtracted from the stored voltage. The pixel signal after CDS is buffered by the source follower and connected via switch to common column readout line.

Layouts implemented in the test chip
The test chip is fabricated in 0.35μm technology, pixel pitch size is 25 μm, epi-layer thickness 20 μm. In order to achieve better MAPS performances, both the geometry of the charge collecting diode and the amplifier design is considered in the optimization process. Two different well diode shapes were tested: square and L-shaped.

Measurement with Spectre
The layout is simulated with Spectre, with parasitic capacitances extracted. The amplifier and CDS circuit are powered during 160 ns, which defines pixel readout time. The integration time, or time between two successive pixel readouts is 160 μs. The temperature is set to 20°C.

Charge collection efficiency simulation
The charge collection efficiency (CCE) is simulated with the device simulator ISE-TCAD for different size of square well and thickness of epitaxial layer. Two ways of doping of the epitaxial layer are tested: uniformly doped and gradually doped (graded).

The influence of graded (right, p doping gradually decreases in positive x direction) on the excess of electrons concentration (after 19 ns of m.i.p. crossed the epitaxial layer) decreases slower in case of uniformly doped substrate (left), and the spread will be larger.

Conclusions
Few amplifier circuits are proposed, designed and tested. The signal-to-noise ratio is maximized by optimizing transistor parameters for different size of charge collection diode. Best SNR(= 23) is obtained for improved cascode with feedback and square well 4.5 μm. The L-shaped well also shows good signal-to-noise ratio of 15 for all amplifier circuits. For the same L-shaped diode, the amplifiers with time variant feedback and time invariant feedback have similar SNR of 15. The charge collection efficiency in the seed pixel can be improved by almost factor of two by using L-shaped well, however signal-to-noise ratio decreases, due to capacitor increase. The simulation of different epi-layer thickness and graded epi-layer shows increase of charge collection efficiency for smaller thickness and the graded substrate has always superior charge collection efficiency.