Improved radiation tolerance of MAPS using a depleted epitaxial layer

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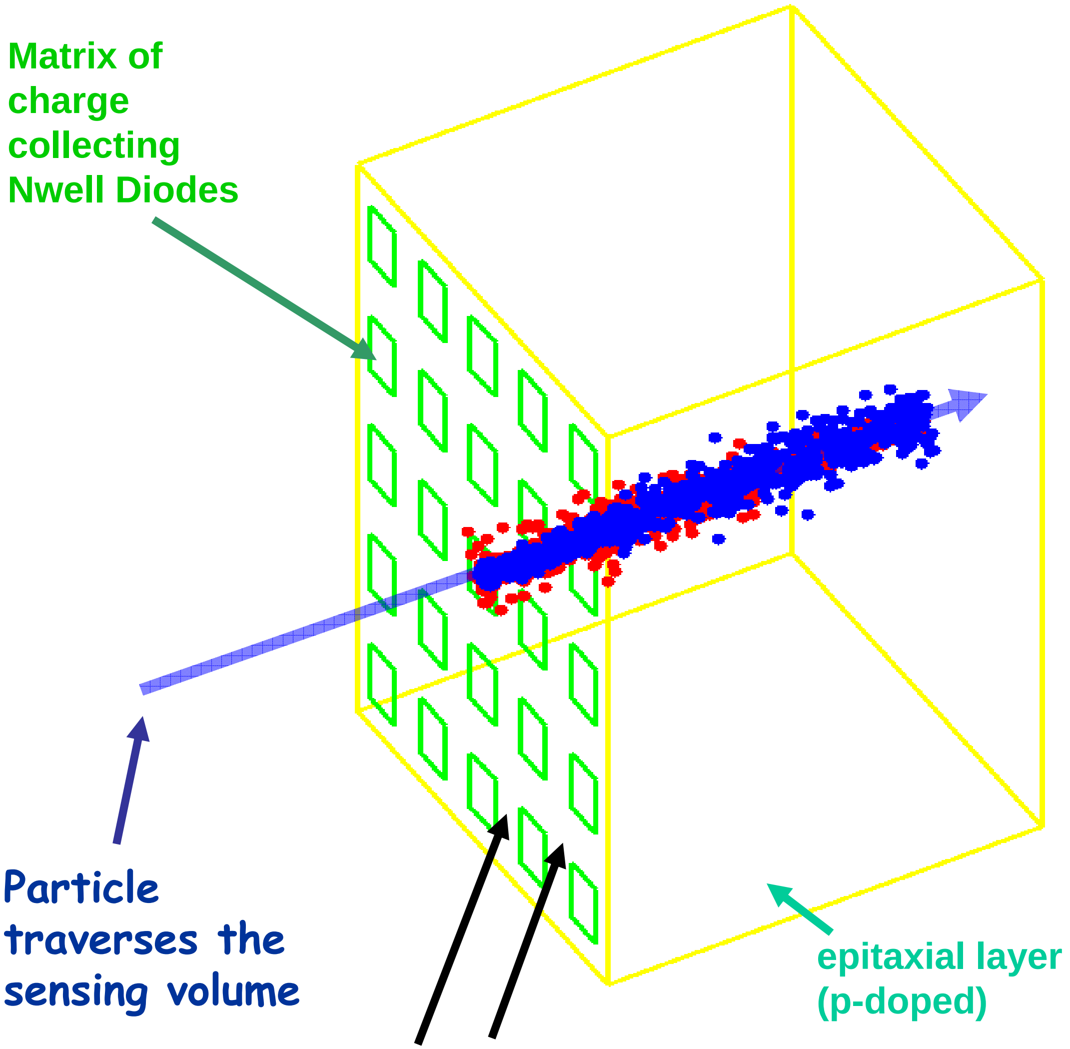
- Mimosa25 sensor prototype implemented in a high resistivity epitaxial layer, which improves radiation tolerance

- Calibration, tests with ^{106}Ru and results for the irradiated sensors

- Conclusions and perspectives

Monolithic Active Pixel Sensors



Readout circuits - standard CMOS technology

Under development since 1999 at IPHC (Strasbourg):

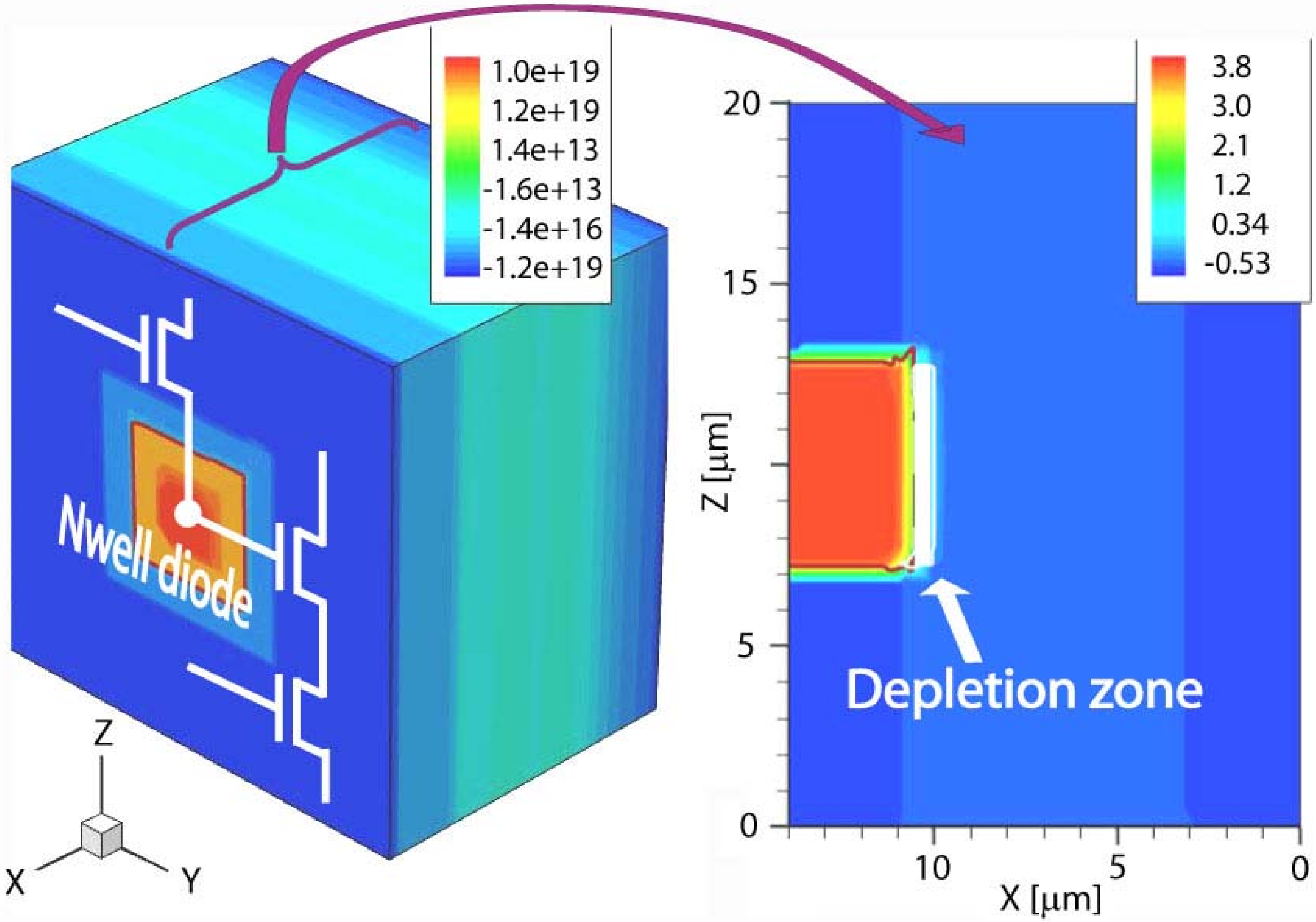
1. MAPS implemented in standard CMOS substrate with readout electronics
2. use p-epitaxial layer as sensing volume (~10-20 µm)
3. Nwell Diodes collect e-h pair liberated by the particle

⬇

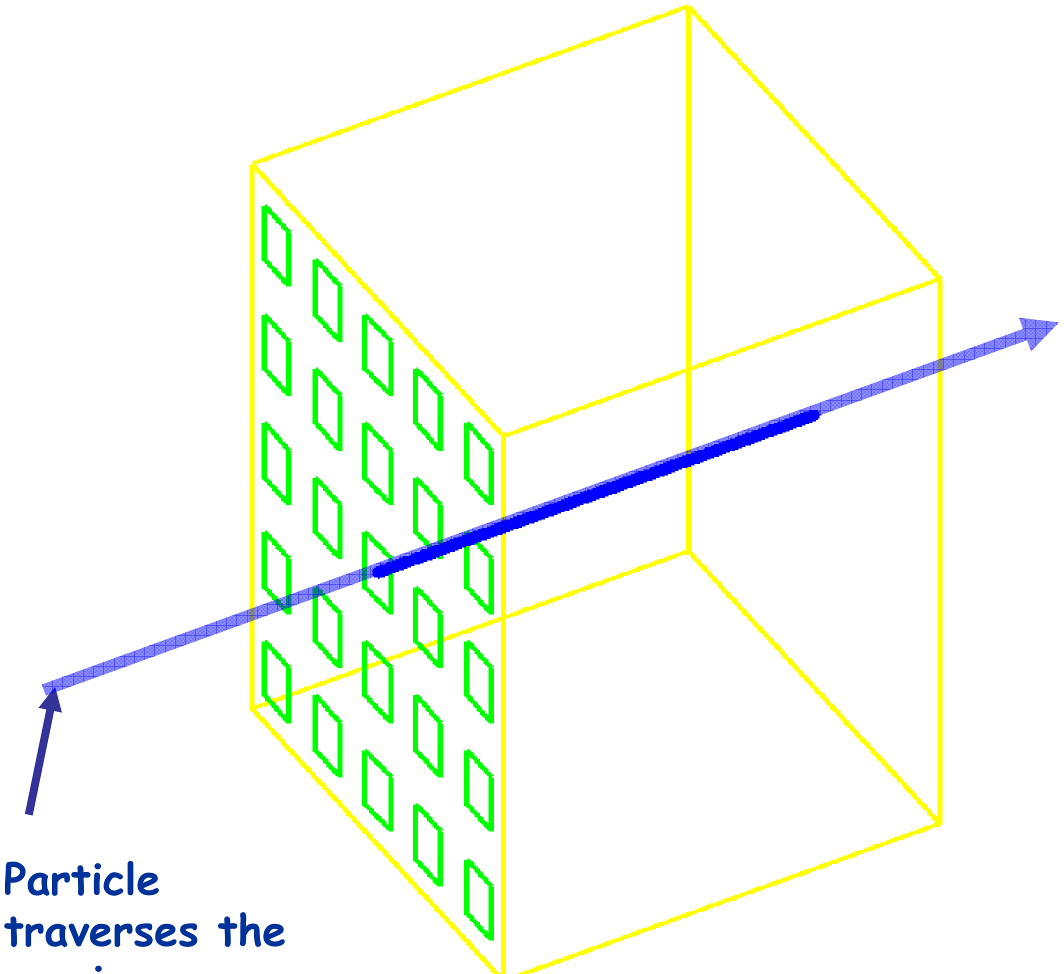
- low cost
- high granularity
- low material budget
- in-pixel signal amplification
- low noise
- integrated readout and signal processing

MAPS implemented in standard CMOS technology

standard CMOS technology p-epitaxial layer has low resistivity ~10 Ω cm



MAPS: charge collection



Blue: electrons
Red: holes

Particle traverses the sensing volume

MAPS: tolerance to non-ionising radiation

1. charge collection is large (>100 ns) because of not depleted P-epi
2. non-ionising radiation create traps

optimization of the pitch size, Nwell diode size

But: signal-to-noise ratio drops down to ~15 after fluence of the order 10^{13} n_{eq}/cm^2

optimise doping of the p-epitaxial layer...

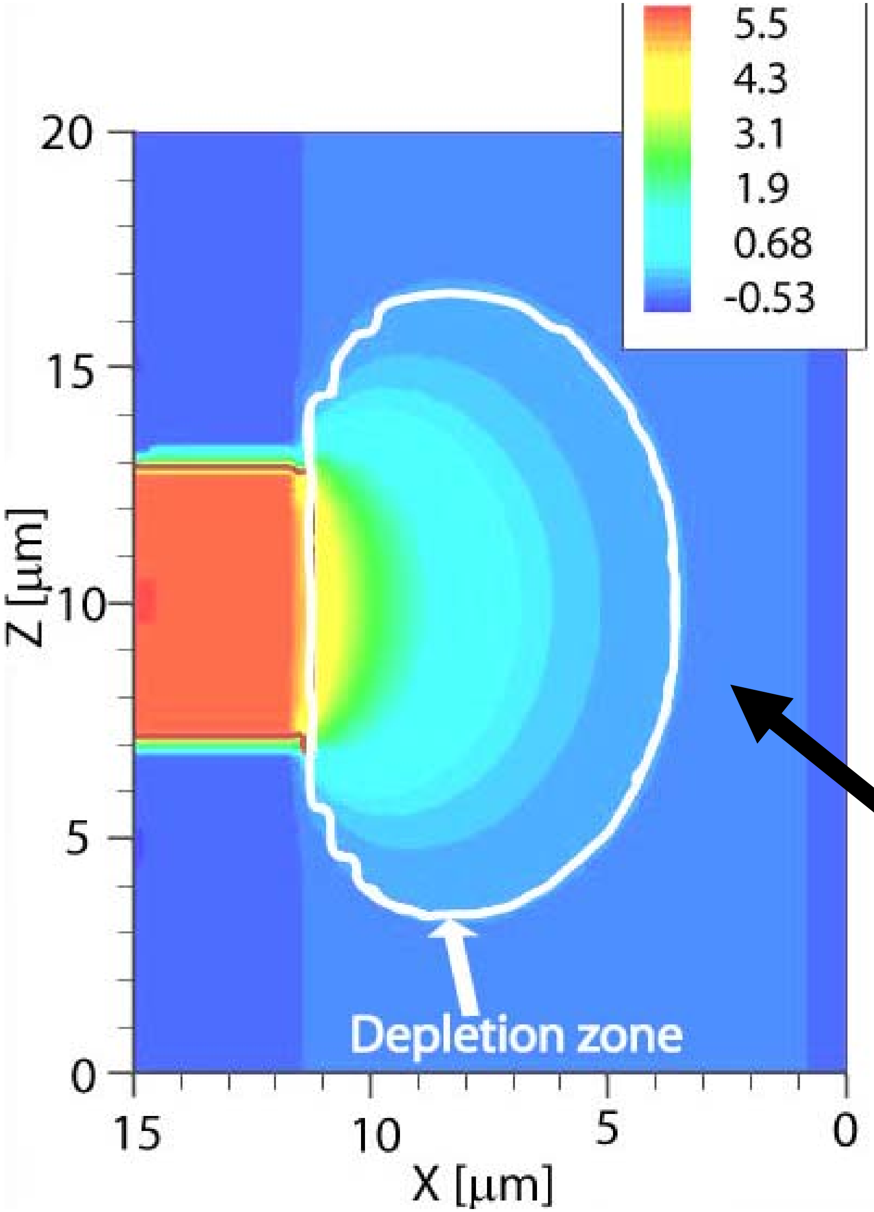
MAPS: improving tolerance to non-ionising radiation

The technology optimisation is very expensive...
but if there are some common problems has to be solved for
commercial applications, one can try to use it..

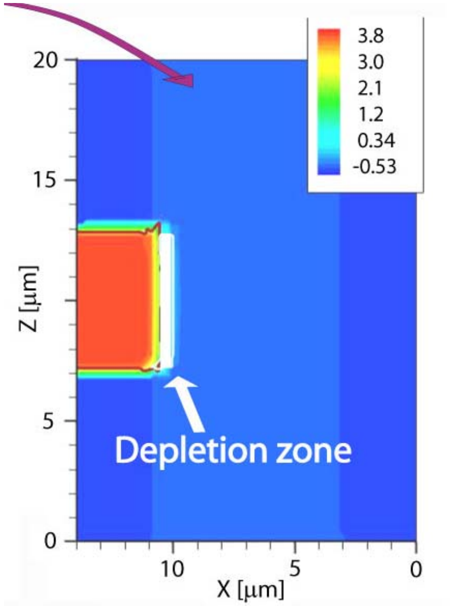
the need of industry for improvement of the photo-sensing elements embedded in to CMOS chip led
to replacing low resistivity (~10 Ω cm) epitaxial layer by relatively high resistivity thin epitaxial layer (~1000 Ω cm), and this was commercially available as an options for standard 0.6 μm process

this layer should be possible to deplete at standard CMOS voltages (<5V)

TCAD Simulations: MAPS in a high resistivity epitaxial layer



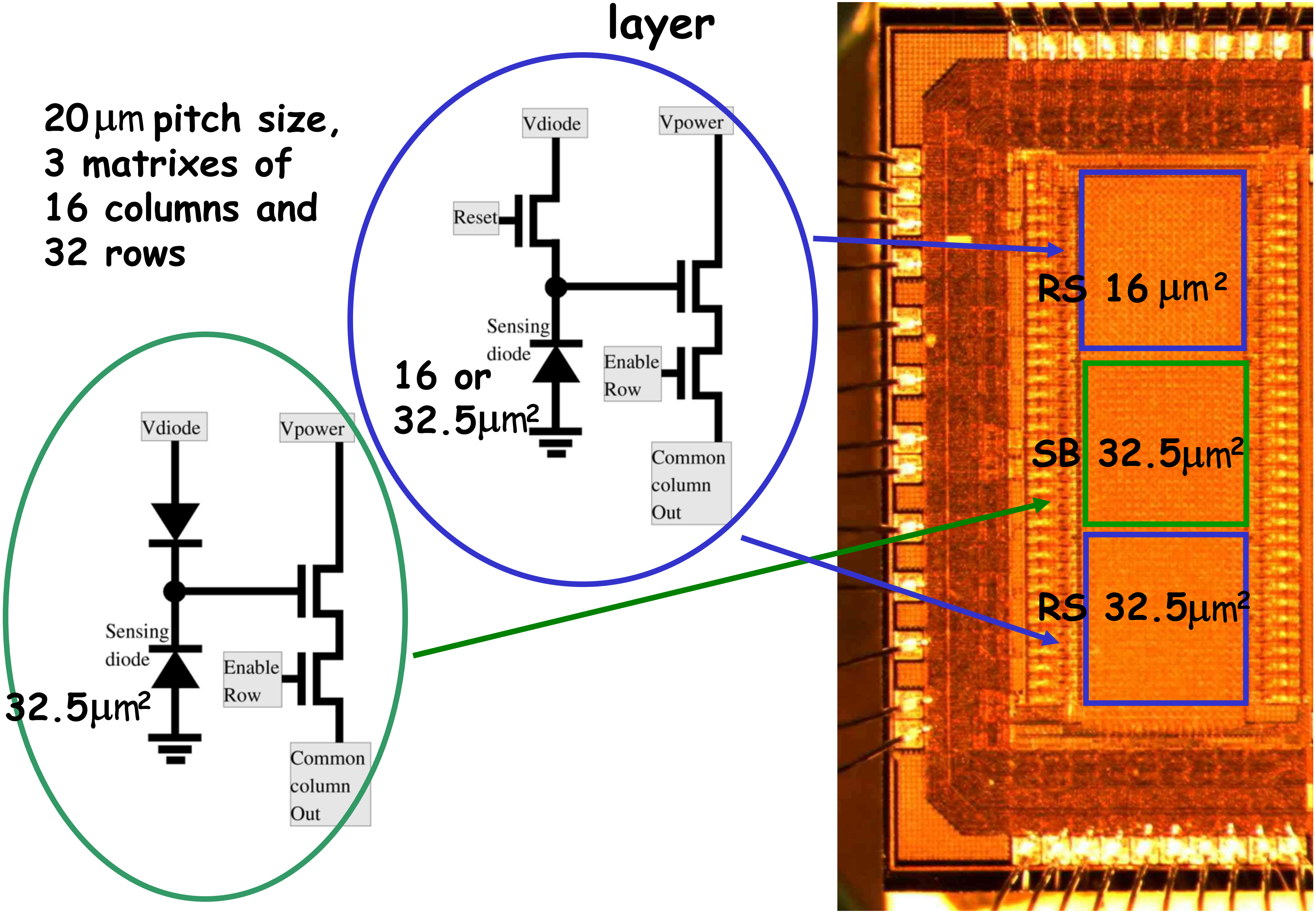
For comparison: standard CMOS technology, low resistivity P-epi



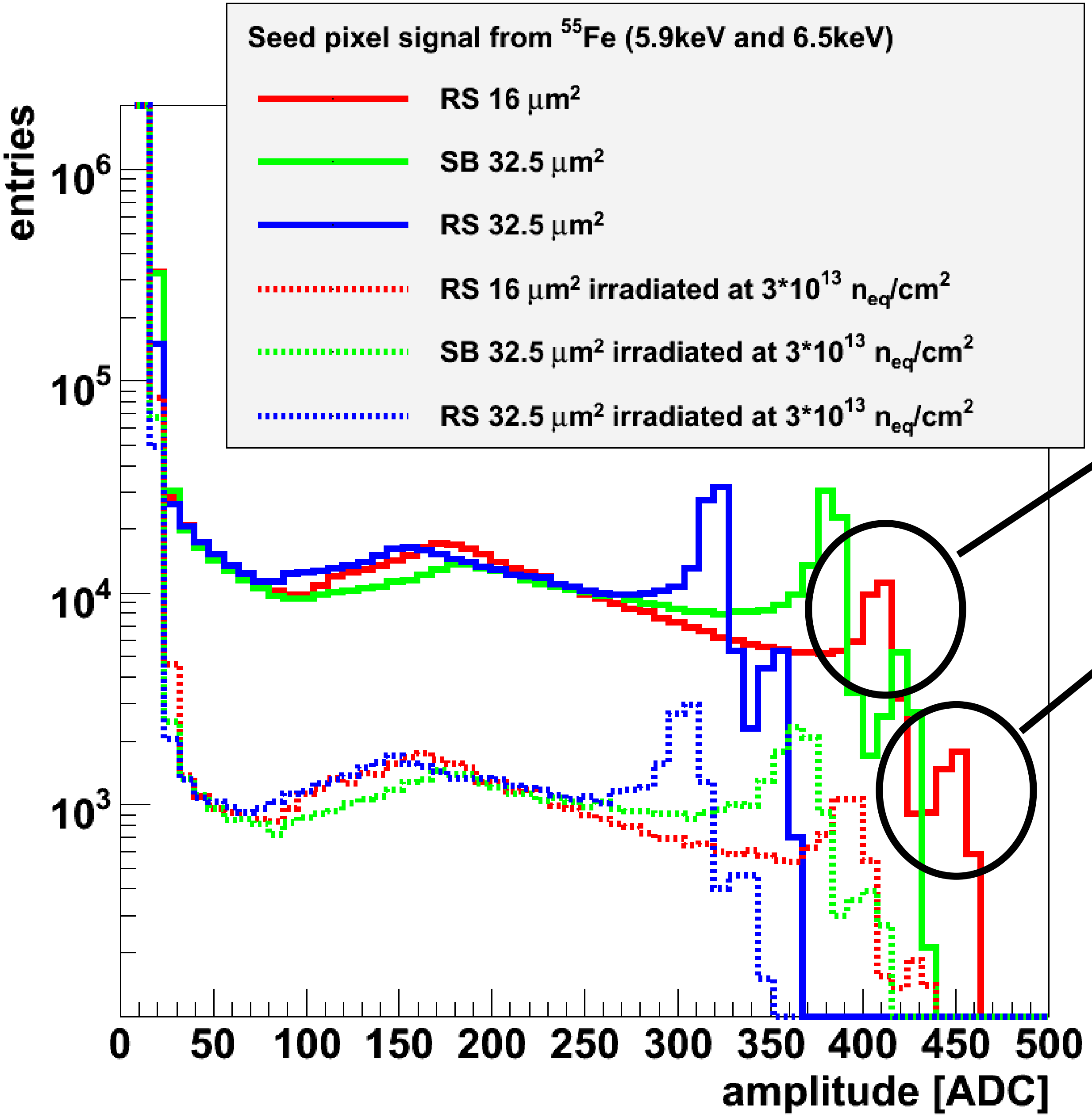
high resistivity P-epi: size of depletion zone size is comparable to the P-epi thickness!

Mimosa25 sensor prototype in a high resistivity epitaxial layer

20 µm pitch size,
3 matrixes of
16 columns and
32 rows



Mimosa25: calibration with ^{55}Fe

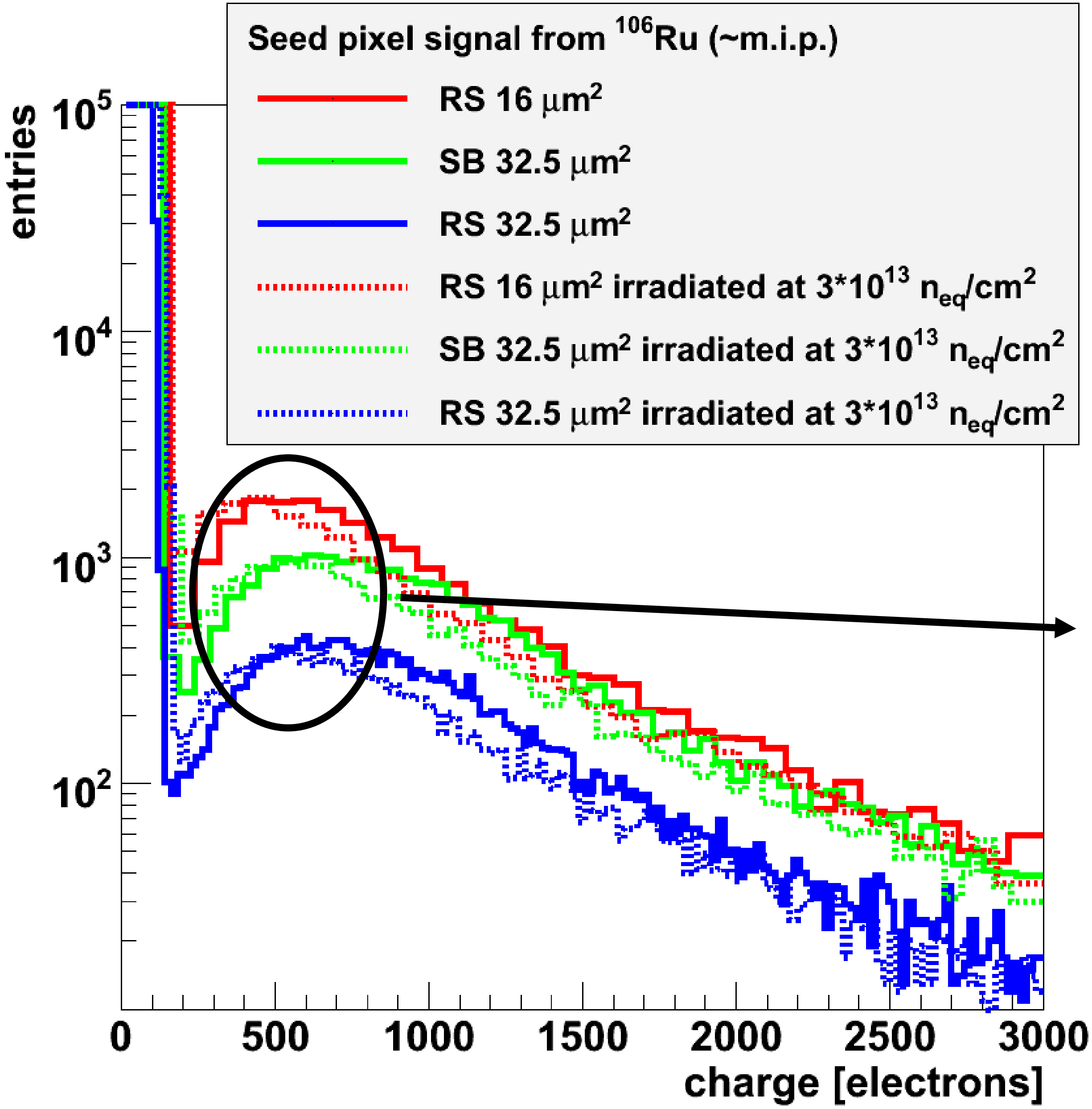


5.9 keV converted to charge carriers near Nwell Diode: used to calibrate readout gain

6.5 keV

temperature
20 C^O

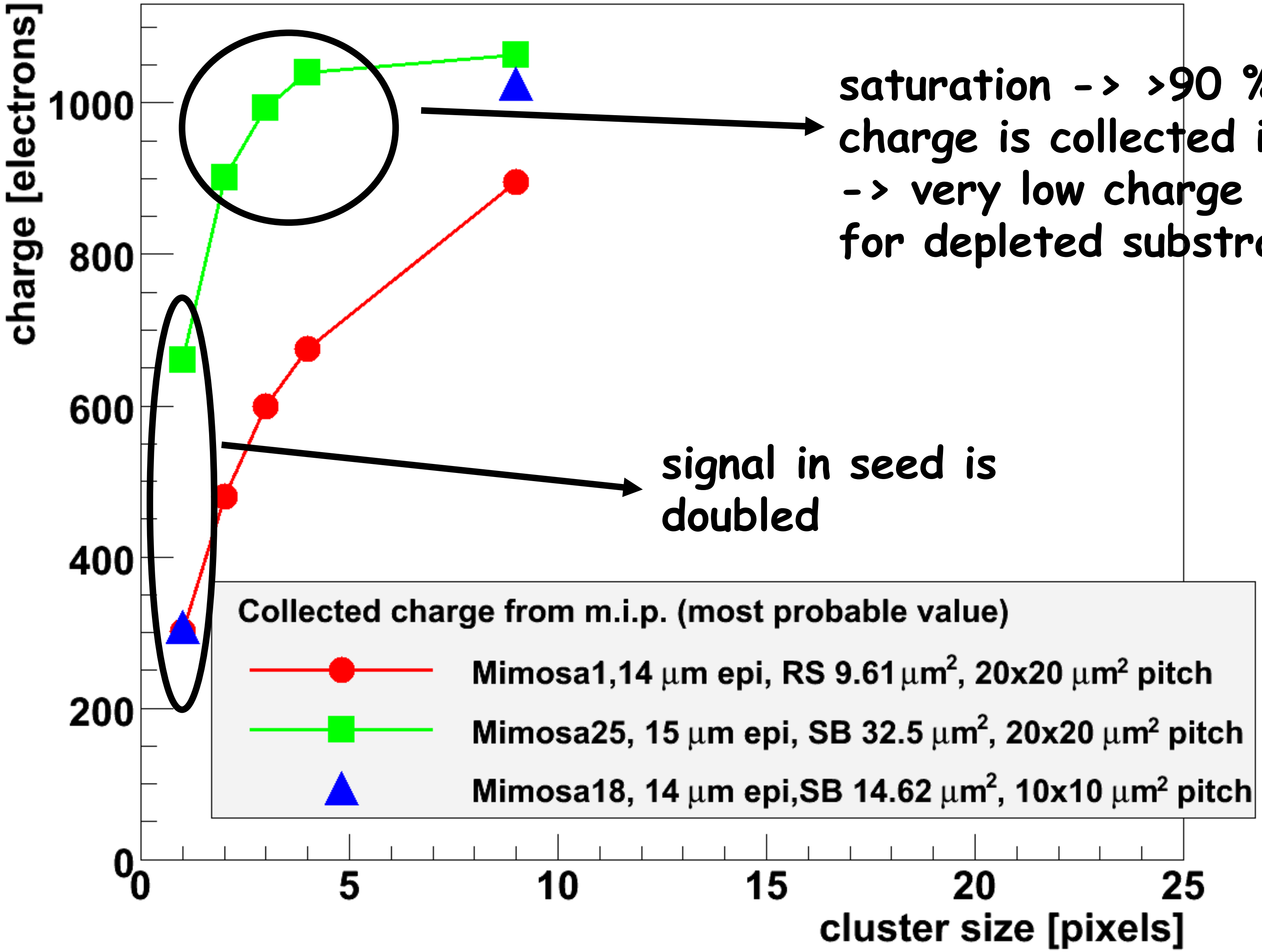
Mimosa25: measurements with ^{106}Ru



Landau distribution m.p.v., used to evaluate the sensors for to m.i.p.

temperature
20 C^O

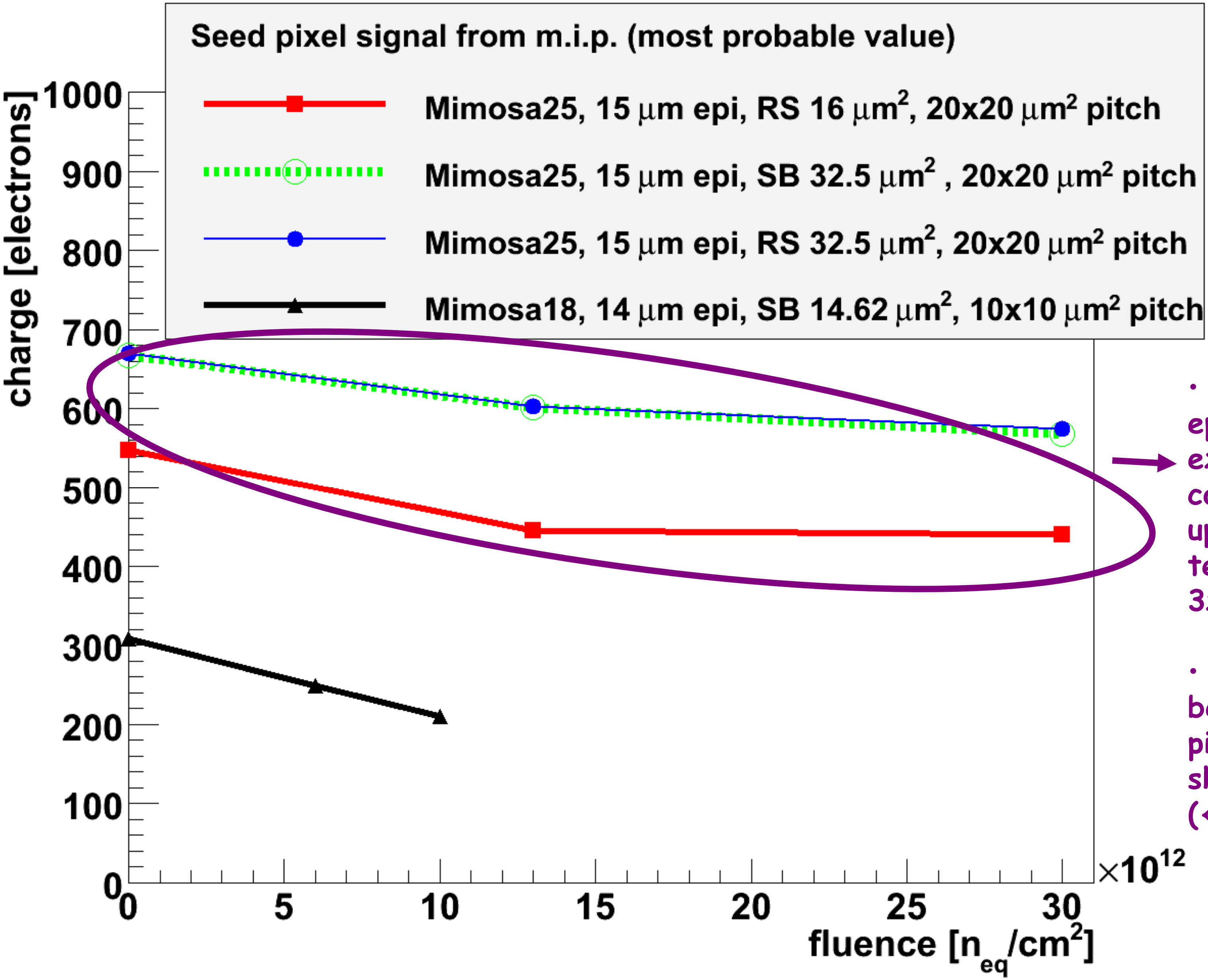
Charge collection and charge sharing comparison for non-irradiated sensors



saturation -> >90 % of charge is collected is 3 pixels -> very low charge spread for depleted substrate

signal in seed is doubled

Comparison of charge collection for irradiated sensors



- For depleted epitaxial layer the excellent charge collection maintained up to the maximum tested value of 3×10^{13} n_{eq}/cm^2

- Results from test beam at CERN with pions of 120 GeV/c shows similar values (<10% of difference)

Conclusions

- MAPS can profit from using resent commercially available CMOS process developed for embedded in chip photodiodes : high resistivity depleted epitaxial layer

- Mimosa25 sensor MAPS prototype was implemented first time in a high resistivity epitaxial layer

- The sensor was calibrated and tested with m.i.p.s

- The signal-to-noise ratio for m.p.v. of landau distribution is about 35 for the Mimosa25 "SB 32.5 μm ^{2}" exposed to a fluence of **3×10^{13} n_{eq}/cm^2**, compared to 14.7 for 0.2x10^{13} **n_{eq}/cm^2** for the low-resistivity epitaxial layer

- The sensors implemented in a depleted epitaxial layer have double signal-to-noise ratio for the fluence of 15 times larger **=>** The limit of radiation tolerance of **MAPS** can be extended by the order of magnitude **up to ~ 10^{14} n_{eq}/cm^2**

Perspectives

- At the moment only 0.6µm technology is commercially available, which may be not sufficient for complex circuitry integrated in MAPS -> 3D integration techniques combining different technologies provide a very attractive solution

- Development of technologies (at least two by now) with a smaller feature size in a similar high resistivity epitaxial layer has been started